Spartan-II™ 200 PCI Development Board User's Guide

Version 1.0
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PN# DS-MANUAL-SPARTANII-200PCI

Memec Design

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1 Overview

The Spartan-II 200 PCI Development Kit provides a complete solution for developing designs and applications based on the Xilinx Spartan-II FPGA family. The kit bundles an expandable Spartan-II based system board with a power supply, user guide and reference designs. Also available from Memec Design, optional P160 expansion modules enable further application specific prototyping and testing. Xilinx ISE software and a JTAG cable are available as kit options.

The Spartan-II system board utilizes the 200,000 gate Xilinx Spartan-II device (XC2S200-6FG456C) in the 456 fine-pitch ball grid array package. The high gate density and large number of user I/Os allows complete system solutions to be implemented in the low cost FPGA. The system board includes two clock sources, a 32-bit PCI edge connector, 8MB SDRAM memory, an RS-232 port, LED displays, switches and additional user support circuits. The board supports the Memec Design P160 expansion module standard, which allows application-specific expansion modules to be easily added.

The Spartan-II FPGA family has the advanced features needed to fit the most demanding, high volume applications. The Spartan-II 200 PCI Development Kit provides an excellent platform to explore these features so that you can quickly and effectively meet your time-to-market requirements.

2 The Spartan-II Development Board

The Spartan-II Development Board provides the FPGA, PCI edge connector, support circuits and the P160 expansion slot for a complete system-level design. Figure 1 shows a picture of the board and its features.

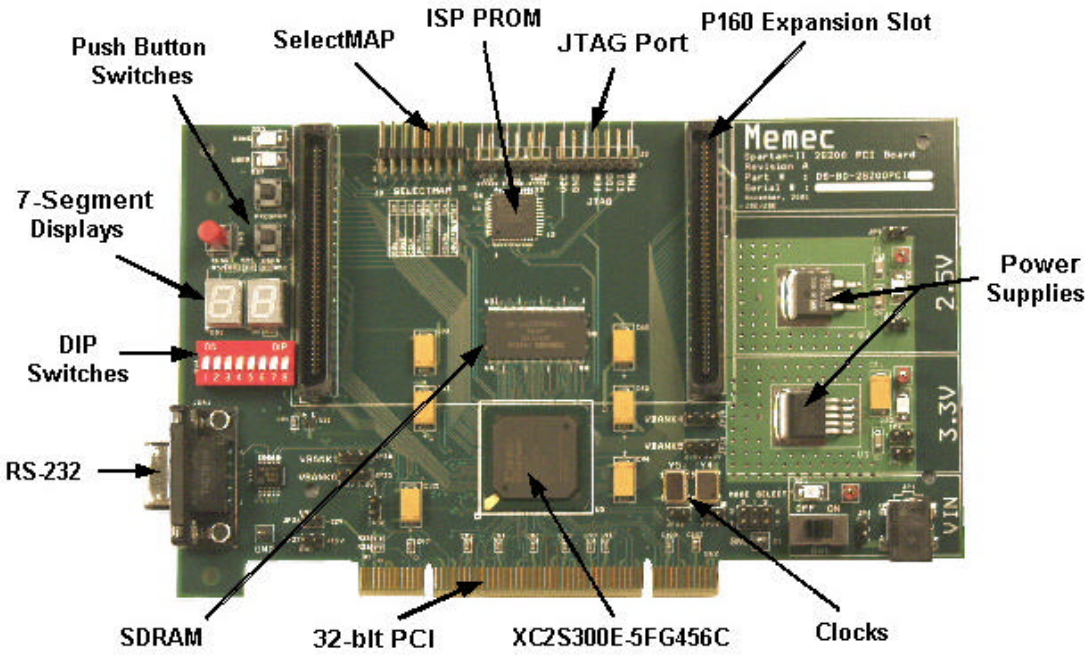


Figure 1 – Spartan-II Development Board

3 Spartan-II Development Board Features

A high-level block diagram of the Spartan-II 200 PCI development board is shown in Figure 2 followed by a brief description of each sub-section.

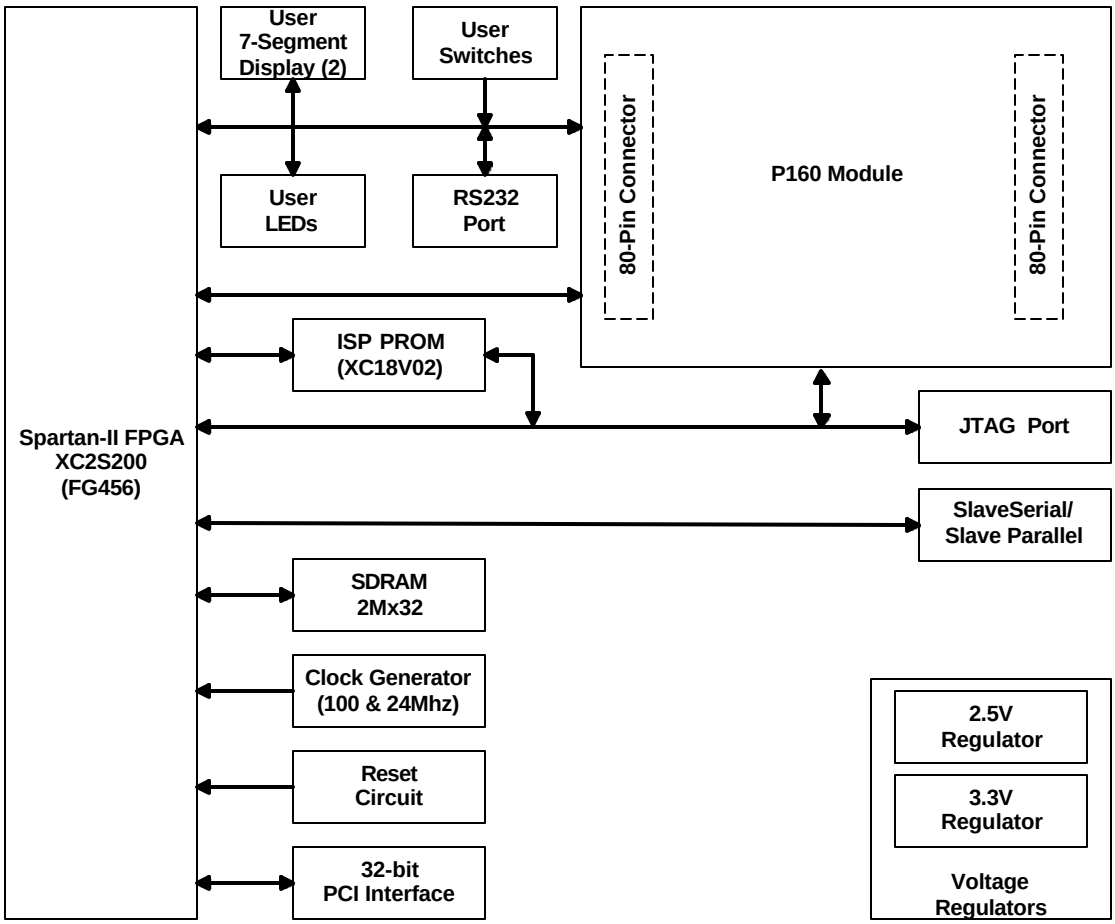


Figure 2 - Spartan-II 200 PCI Development Board Block Diagram

3.1 SDRAM Memory

The Spartan-II 200 PCI development board provides 8MB of SDRAM memory. This memory is implemented using the Toshiba TC59S6432CFT 2Mx32 SDRAM (or a compatible) device. A high-level block diagram of the SDRAM interface is shown below followed by a table describing the SDRAM memory interface signals.

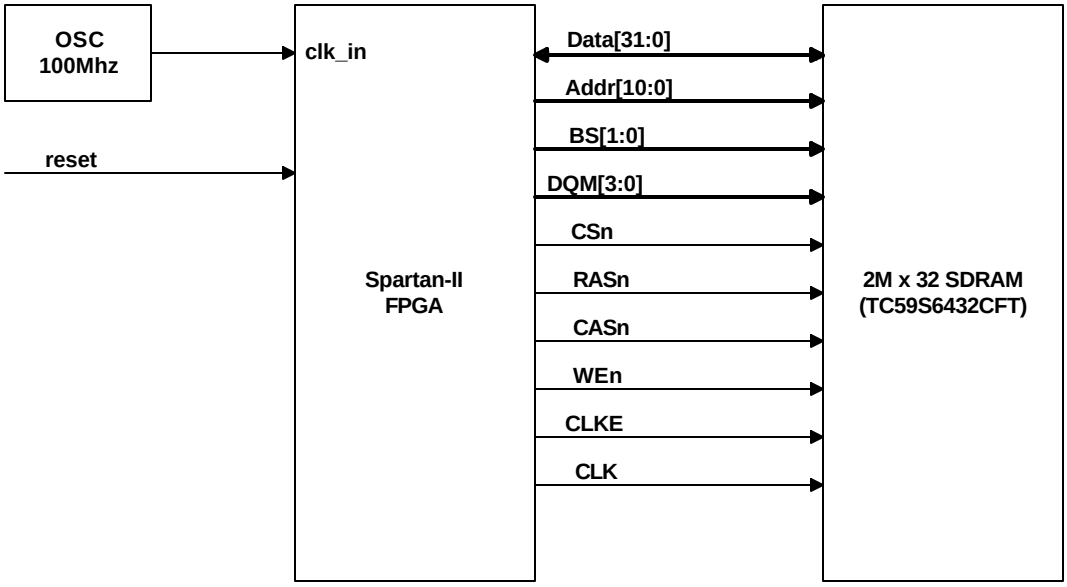


Figure 3 – SDRAM Interface

Table 1 – SDRAM Interface Signal Description

Signal Name	Description	FPGA Pin #	SDRAM Pin #
A0	Address 0	M18	25
A1	Address 1	L18	26
A2	Address 2	L20	27
A3	Address 3	J21	60
A4	Address 4	J22	61
A5	Address 5	K21	62
A6	Address 6	K22	63
A7	Address 7	L21	64
A8	Address 8	L22	65
A9	Address 9	M22	66
A10	Address 10	M19	24
DQ0	Data 0	T18	2
DQ1	Data 1	W22	4
DQ2	Data 2	R18	5
DQ3	Data 3	P18	7
DQ4	Data 4	V20	8
DQ5	Data 5	U19	10
DQ6	Data 6	U20	11
DQ7	Data 7	T19	13
DQ8	Data 8	P22	74
DQ9	Data 9	P21	76
DQ10	Data 10	R22	77
DQ11	Data 11	T21	79
DQ12	Data 12	U22	80
DQ13	Data 13	U21	82
DQ14	Data 14	V22	83
DQ15	Data 15	V21	85

DQ16	Data 16	J20	31
DQ17	Data 17	J19	33
DQ18	Data 18	H19	34
DQ19	Data 19	G20	36
DQ20	Data 20	G19	37
DQ21	Data 21	F20	39
DQ22	Data 22	F19	40
DQ23	Data 23	E20	42
DQ24	Data 24	C22	45
DQ25	Data 25	D21	47
DQ26	Data 26	D22	48
DQ27	Data 27	E21	50
DQ28	Data 28	E22	51
DQ29	Data 29	F21	53
DQ30	Data 30	F22	54
DQ31	Data 31	G21	56
BS0	Bank Select 0	N20	22
BS1	Bank Select 1	M20	23
DQM0	Write Mask	T20	16
DQM1	Write Mask	N21	71
DQM2	Write Mask	K19	28
DQM3	Write Mask	H21	59
CSn	Chip Select	N19	20
RASn	Row Address Strobe	P20	19
CASn	Column Address Strobe	P19	18
WEn	Write Enable	R19	17
CLK	Clock	N18	68
CKE	Clock Enable	N22	67

3.2 Clock Generation

The Spartan-II development board provides three master clock inputs to the Spartan-II FPGA. The following table provides a brief description of these clock signals.

Table 2 - Spartan-II Development Board Master Clocks

Signal Name	Spartan-II Pin #	Direction	Description
CLK.CAN2	Y11	Input	On-board 100 MHz Oscillator
CLK.CAN1	W12	Input	On-board 24 MHz Oscillator
User Clock	A11	Input	User Clock Input via JP30

The Spartan-II development board provides two on-board oscillators running at 100Mhz (CLK.CAN1) and 24Mhz (CLK.CAN2). The 100Mhz oscillator is enabled when the JP24 jumper is open, while leaving the JP32 jumper open will enable the 24Mhz oscillator. In addition to these oscillators, a jumper is provides (JP30) for a User supplied clock input to the FPGA.

JP30 is provided as an external clock input jumper, connecting to the global clock pin on A11 of the FPGA. Pin 1 of JP30 connects to A11 and pin 2 of JP30 connects to ground. The PCI clock from the PCI edge connector connects to the global clock pin on C11 of the FPGA.

3.3 Reset Circuit

The Spartan-II development board uses the TI TPS3125 voltage supervisory device to monitor the Spartan-II FPGA core voltage (2.5V). This circuit asserts a reset signal (RESETn_FPGA, Pin

B10) to the Spartan-II device when the 2.5V core voltage falls below its minimum specifications (V). The reset signal to the FPGA is a fixed 100ms active low pulse. In addition to monitoring the core voltage, this circuit can be used to generate a reset pulse by activating the Master Reset (MRn) signal to the TPS3125 device via the on-board push-button switch (SW3). The following figure shows the reset circuit on the Spartan-II development board.

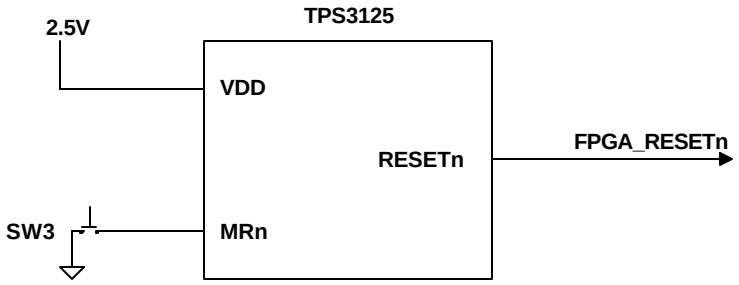


Figure 4 – Reset Circuit

3.4 User 7-Segment Display

The Spartan-II development board utilizes two common-cathode 7-segment LED displays that can be used during the test and debugging phase of a design. The user can turn a given segment on by driving the associated signal high. The following figure shows the user 7-segment display interface to the Spartan-II FPGA.

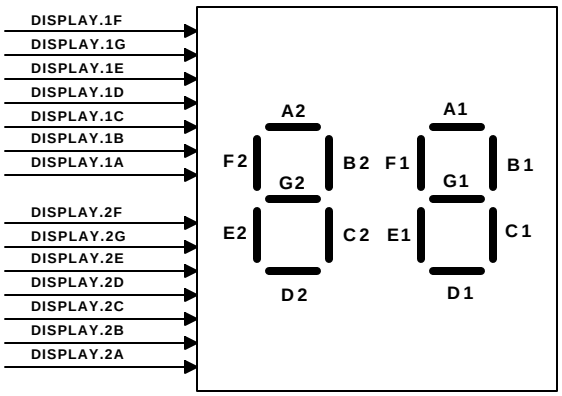


Figure 5 - 7-Segment LED Display Interface

3.4.1 7-Segment Display Signal Description

The following table shows the 7-Segment LED display pin descriptions.

Table 3 - 7-Segment Display Signal Descriptions

Signal Name	Spartan-II Pin #	Description
DISPLAY.1A	E10	7-Segment LED Display1, Segment A
DISPLAY.1B	E9	7-Segment LED Display1, Segment B
DISPLAY.1C	E8	7-Segment LED Display1, Segment C
DISPLAY.1D	E6	7-Segment LED Display1, Segment D
DISPLAY.1E	E7	7-Segment LED Display1, Segment E
DISPLAY.1F	F11	7-Segment LED Display1, Segment F
DISPLAY.1G	E11	7-Segment LED Display1, Segment G
DISPLAY.2A	D6	7-Segment LED Display2, Segment A
DISPLAY.2B	C5	7-Segment LED Display2, Segment B
DISPLAY.2C	D5	7-Segment LED Display2, Segment C
DISPLAY.2D	C7	7-Segment LED Display2, Segment D
DISPLAY.2E	D7	7-Segment LED Display2, Segment E
DISPLAY.2F	C6	7-Segment LED Display2, Segment F
DISPLAY.2G	A8	7-Segment LED Display2, Segment G

3.5 User LED

The Spartan-II development board provides a single user LED. Pin A10 of the Spartan-II FPGA is used to drive this active low signal.

3.6 User Push Button Switch (SW5)

The Spartan-II development board design provides a user push button switch input to the Spartan-II FPGA. The push button switch can be used to generate an active low signal.

3.6.1 User Push Button Switch Signal Assignment

The following table shows the pin assignment for the user push button switch.

Table 4 - User Push Button Switch Signal Assignments

Signal Name	Spartan-II Pin #	Description
PUSH.USER1	B1	User Push Button Switch Input 1 (SW5)

3.7 Program Switch (SW2)

The Spartan-II development board provides a push button switch for initiating the configuration of the Spartan-II FPGA. This switch is used when the XC18V02 ISP PROM configures the Spartan-II FPGA. After programming of the XC18V02 ISP PROM, this switch can assert the PROGn signal. Upon activation of the PROGn signal, the XC18V02 ISP PROM initiates the configuration of the Spartan-II FPGA.

3.8 User DIP Switch (SW4)

The Spartan-II development board provides 8 user switch inputs. These switches can be statically set to a low or high logic level.

3.8.1 User DIP Switch Interface

The following figure shows the user DIP Switch interface to the Spartan-II FPGA.

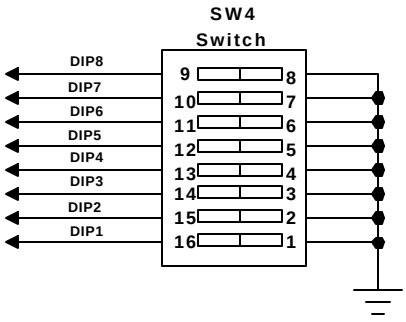


Figure 6 – User DIP Switch Interface

3.8.2 User DIP Switch Signal Assignments

The following table shows the user switch pin assignments.

Table 5 - User DIP Switch Signal Assignments

Signal Name	Spartan-II Pin #	Description
DIP8	E4	User Switch Input 8
DIP7	F3	User Switch Input 7
DIP6	E3	User Switch Input 6
DIP5	F5	User Switch Input 5
DIP4	G5	User Switch Input 4
DIP3	F4	User Switch Input 3
DIP2	C1	User Switch Input 2
DIP1	D2	User Switch Input 1

3.9 RS232 Port

The Spartan-II development board provides an RS232 port that can be driven by the Spartan-II FPGA. A subset of the RS232 signals is used on the Spartan-II development board to implement this interface (RD and TD signals).

3.9.1 RS232 Interface

The Spartan-II development board provides a DB-9 connection for a simple RS232 port. This board utilizes the TI MAX3221 RS232 driver for driving the RD and TD signals. The user provides the RS232 UART code, which resides in the Spartan-II FPGA.

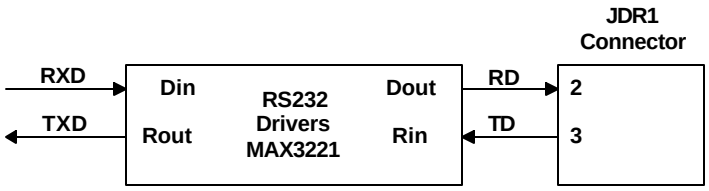


Figure 7 – RS232 Interface

3.9.2 RS232 Signal Descriptions

The following table shows the RS232 signals and their pin assignments to the Spartan-II FPGA.

Table 6 - RS232 Signal Descriptions

Signal Name	Spartan-II Pin #	Description
RXD	B9	Received Data, RD
TXD	A9	Transmit Data, TD

3.10 JTAG Port

The Spartan-II development board design provides a JTAG port that can be used to configure and/or program various devices on the board and JTAG devices located on the P160 module.

3.10.1 JTAG Connector

The Spartan-II development board provides a JTAG connector that can be used to program the on-board ISP PROM, configure the Spartan-II FPGA, and program and/or configure JTAG devices located on the P160 module. The following figure shows the pin assignments for the JTAG connector on the Spartan-II development board.

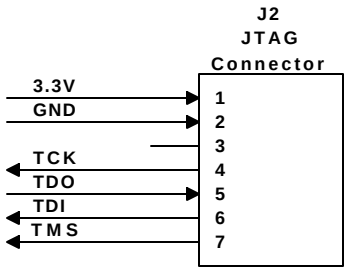


Figure 8 – JTAG Connector

3.10.2 JTAG Signal Descriptions

The following table provides a brief description of the JTAG signals and their pin assignments to the Spartan-II FPGA.

Table 7 - JTAG Signal Descriptions

Signal Name	Description
TDI	JTAG Data Input
TCK	JTAG Clock Input
TMS	JTAG Test Mode Input
TDO	JTAG Data Output

3.10.3 JTAG Chain

The following figure shows the JTAG chain on the Spartan-II development board. If any of the devices in the chain are not populated, its associated jumper must be closed in order to maintain the chain integrity. If the P160 module is not present, then jumper JP25 must be closed in order to connect the P160 module TDI pin to its TDO pin.

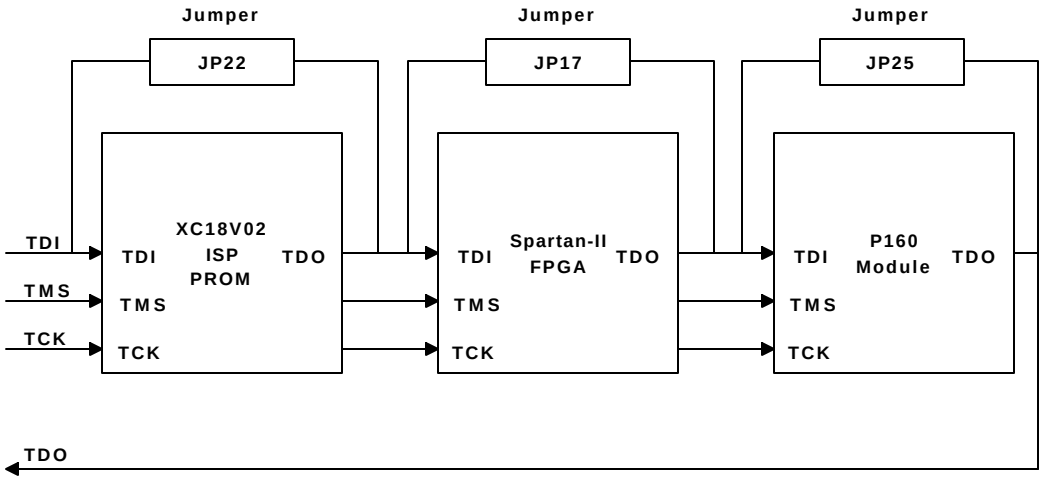


Figure 9 – Spartan-II Development Board JTAG Chain

3.10.4 JTAG Chain Jumper Settings

The following table shows the JTAG chain jumper setting on the Spartan-II development board.

Table 8 - JTAG Chain Jumper Settings

Jumper	Setting	Description
JP22	Open	XC18V02 ISP PROM is present
	Closed	XC18V02 ISP PROM is not present
JP17	Open	Spartan-II FPGA is present
	Closed	Spartan-II FPGA is not present
JP25	Open	P160 module is present
	Closed	P160 module is not present

3.11 Slave Parallel/Slave Serial Port

In addition to the JTAG mode, the Spartan-II FPGA on the Spartan-II development board can be configured using the Slave Serial or the Slave Parallel mode of configuration. The following figure shows the connector pin assignments for the Slave Serial/Slave Parallel port.

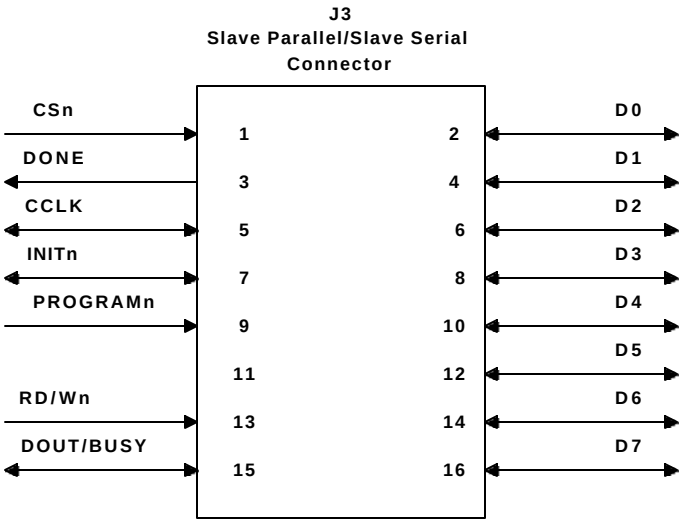


Figure 10 – Slave Parallel/Slave Serial Connector

3.11.1 Slave Parallel

In the Slave Parallel configuration mode, a byte of configuration data is loaded into the Spartan-II FPGA during each CCLK clock cycle. In this mode, an external source drives the CCLK clock and the data bus containing the configuration data. The following figure shows the Slave Parallel configuration mode interface to the Spartan-II FPGA. **The JP12 jumper must be installed in position 1-2 for this mode of configuration.**

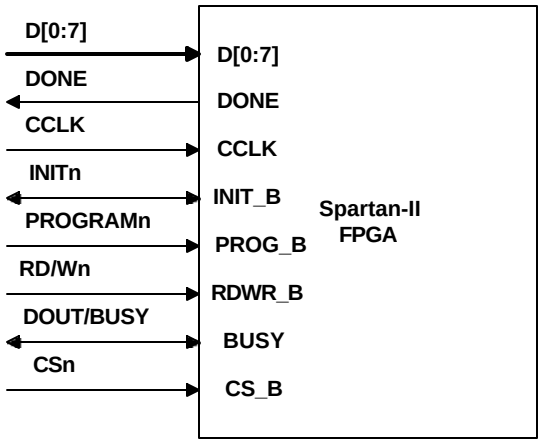


Figure 11 – Slave Parallel Mode Configuration

3.12 Slave Serial Port

In the Slave Serial configuration mode, a bit of configuration data is loaded into the FPGA during each CCLK clock cycle. In this mode, an external source places the most significant bit of each byte on the DIN pin first and then drives the CCLK clock to store data into the FPGA. The following figure shows the Slave Serial configuration mode interface to the Spartan-II FPGA. **The JP12 jumper must be installed in position 1-2 for this mode of configuration.**

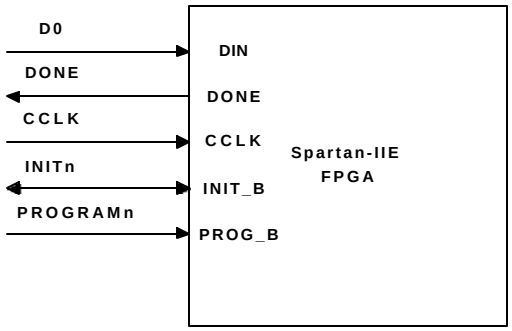


Figure 12 – Slave Serial Mode Configuration

3.13 Bank I/O Voltage

The Spartan-II development board allows the Spartan-II I/O pins to be configured for 2.5V or 3.3V operation. All Spartan-II user I/O pins are grouped in 8 different banks. Each bank of I/O pins on the board can be configured to operate in the 2.5V or the 3.3V mode.

3.13.1 Bank I/O Voltage Jumper Settings

The following table shows the jumper settings for the Spartan-II bank I/O voltage (VCCO) selection. Each bank can be set to 2.5V or 3.3V.

Table 9 - Bank I/O Voltage Jumper Settings

Bank #	Jumper		I/O Voltage
	JP35		
	1-2	2-3	
	Closed	Open	3.3V
0	Open	**Closed**	2.5V
	JP26		
	1-2	2-3	
	Closed	Open	3.3V
1	Open	**Closed**	2.5V
2	**FIXED**		3.3V
3	**FIXED**		3.3V
	JP19		
	1-2	2-3	
	Closed	Open	3.3V
4	Open	**Closed**	2.5V
	JP34		
	1-2	2-3	
	Closed	Open	3.3V
5	Open	**Closed**	2.5V
6	**FIXED**		3.3V
7	**FIXED**		3.3V

3.14 ISP PROM

The Spartan-II development board utilizes the Xilinx XC18V02 ISP PROM, allowing FPGA designers to quickly download revisions of a design and verify the design changes in order to meet the final system-level design requirements. The XC18V02 ISP PROM uses two interfaces to accomplish the configuration of the Spartan-II FPGA.

The JTAG port on the XC18V02 device is used to program the PROM with the design bit file. Once the XC18V02 has been programmed, the user can configure the Spartan-II device in the Master Serial mode. The configuration of the Spartan-II device is initiated by asserting the PROGn signal. Upon activation of the PROGn signal (by pressing the SW2 switch), the XC18V02 device will use its FPGA Configuration Port to configure the Spartan-II FPGA.

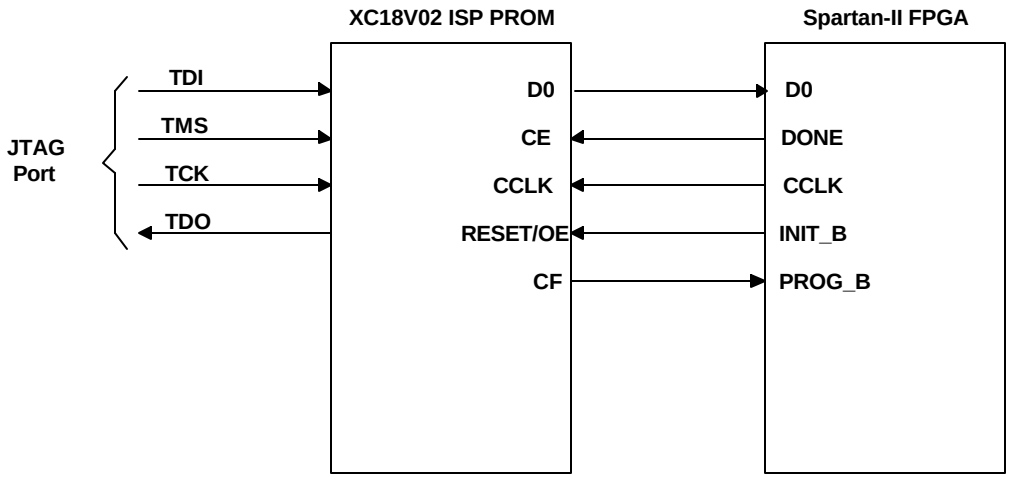


Figure 13 – ISP PROM Interface

3.15 PCI Interface

The Spartan-II 200 PCI development board provides a 32-bit PCI interface edge connector for prototyping PCI-based designs. The Xilinx PCI32 core can be used to implement this interface.

3.15.1 PCI Interface Signal Descriptions

The following table shows the PCI interface signals and their assignments to the Spartan-II FPGA.

Table 10 – PCI Interface Signal Descriptions

FPGA Pin #	JE1 Signal Name	JE1 Pin #		JE1 Signal Name	FPGA Pin #
		A1	B1	**-12V**	
	+12V	A2	B2		
		A3	B3	**GND**	
	TDI	A4	B4	TDO	
	+5V	A5	B5	**+5V**	
M3	INITAn	A6	B6	**+5V**	
		A7	B7		

	+5V	A8	B8		
		A9	B9		
		A10	B10		
		A11	B11		
		A12	B12		
		A13	B13		
		A14	B14		
E2	RSTn	A15	B15	**GND**	
		A16	B16	PCI.CLK	C11
L5	GNTn	A17	B17	**GND**	
	GND	A18	B18	REQn	K2
		A19	B19		
G4	AD30	A20	B20	AD31	E1
		A21	B21	AD29	G3
H5	AD28	A22	B22	**GND**	
F1	AD26	A23	B23	AD27	F2
	GND	A24	B24	AD25	H4
G1	AD24	A25	B25		
L6	IDSEL	A26	B26	C/BE3n	N2
		A27	B27	AD23	H3
H2	AD22	A28	B28	**GND**	
H1	AD20	A29	B29	AD21	J4
	GND	A30	B30	AD19	J5
J2	AD18	A31	B31		
J1	AD16	A32	B32	AD17	J3
		A33	B33	C/BE2n	N3
M6	FRAMEn	A34	B34	**GND**	
	GND	A35	B35	IRDYn	L3
M1	TRDYn	A36	B36		
	GND	A37	B37	DEVSELn	L1
L4	STOPn	A38	B38	**GND**	
		A39	B39		
		A40	B40	PERRn	N5
		A41	B41		
	GND	A42	B42	SERRn	M4
P2	PAR	A43	B43		
K5	AD15	A44	B44	C/BE1n	N4
		A45	B45	AD14	K1
K3	AD13	A46	B46	**GND**	
P4	AD11	A47	B47	AD12	K4
	GND	A48	B48	AD10	R1
P5	AD09	A49	B49	**GND**	
		A50	B50		
		A51	B51		
P1	C/BE0n	A52	B52	AD08	P3
		A53	B53	AD07	R2
T1	AD06	A54	B54		
T2	AD04	A55	B55	AD05	R4
	GND	A56	B56	AD03	U1
R5	AD02	A57	B57	**GND**	
T5	AD00	A58	B58	AD01	V1
		A59	B59		
		A60	B60		
	+5V	A61	B61	**+5V**	
	+5V	A62	B62	**+5V**	

3.16 Voltage Regulators

The following figure shows the voltage regulators that are used on the Spartan-II development board to provide various on-board voltage sources. As shown in the figure, JP1 connector is used to provide the main 5.0V voltage to the board. This voltage source is provided to all on-board regulators to generate the 2.5V, and 3.3V voltages.

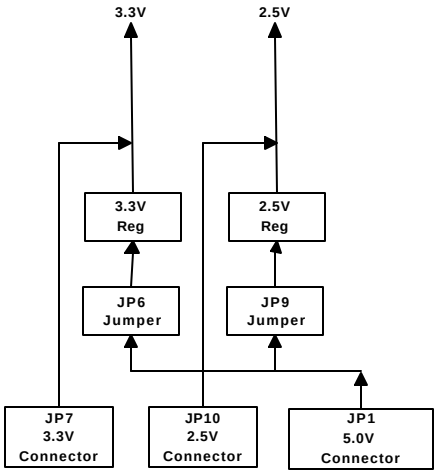


Figure 14 – Spartan-II Development Board Voltage Regulators

For any one of the on-board voltages (2.5V, and 3.3V), if the current provided by the on-board regulator is not sufficient for some applications, the user can directly drive the voltage source and bypass the on-board regulators. This can be accomplished by removing jumpers JP6 and JP9 for 3.3V and 2.5V voltages respectively.

3.16.1 Voltage Regulators Jumper Settings

The following table shows the jumper setting for the 3.3V and 2.5V supply voltages on the Spartan-II PCI development board.

Table 11 - Voltage Regulators Jumper Settings

Jumper	Jumper Setting	3.3V Source	2.5V Source
JP6	Open	External 3.3V supply via JP7 connector	NA
	Closed	On-board 3.3V regulator	NA
JP9	Open	NA	External 2.5V supply via JP10 connector
	Closed	NA	On-board 2.5V regulator

3.17 Spartan-II Configuration Mode Select

The following table shows the Spartan-II Configuration Mode Select jumper settings.

Table 12 - Spartan-II Configuration Mode Select

Mode	PC Pull-up	J1		
		1-2 (M0)	3-4 (M1)	5-6 (M2)
Master Serial	No	Closed	Closed	Closed
Master Serial	Yes	Closed	Closed	Open
Slave Serial	No	Open	Open	Open
Slave Serial	Yes	Open	Open	Closed
Slave Parallel	No	Closed	Open	Open
Slave Parallel	Yes	Closed	Open	Closed
JTAG	No	Open	Closed	Open
JTAG	Yes	Open	Closed	Closed

3.18 P160 Expansion Module

A versatile expansion slot is implemented on the Spartan-II board, allowing application specific cards or modules to be easily interfaced with the Spartan-II FPGA. The P160 Expansion Slot is made up of two 80-pin connectors yielding 110 user I/O signals to an add-on module.

3.18.1 Expansion Module Signal Assignments

The following tables show the Spartan-II pin assignments to the P160 Expansion Module connectors (JX1 & JX2) located on the Spartan-II development board.

Table 13 – JX1 User I/O Connector

FPGA Pin #	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	FPGA Pin #
	TCK	A1	B1	FPGA.BITSTREAM	
NA	**GND**	A2	B2	SM.DOUT/BUSY	
	TMS	A3	B3	FPGA.CCLK	
NA	**Vin**	A4	B4	DONE	
NA	TDI	A5	B5	INITn	
NA	**GND**	A6	B6	PROGRAMn	
NA	TDO	A7	B7	NC	
NA	**3.3V**	A8	B8	LIOB8	B19
E16	LIOA9	A9	B9	LIOB9	A19
NA	**GND**	A10	B10	LIOB10	B18
E15	LIOA11	A11	B11	LIOB11	A18
NA	**2.5V**	A12	B12	LIOB12	B17
E14	LIOA13	A13	B13	LIOB13	A17
NA	**GND**	A14	B14	LIOB14	A16
F12	LIOA15	A15	B15	LIOB15	B15
NA	**Vin**	A16	B16	LIOB16	A15
C10	LIOA17	A17	B17	LIOB17	B14
NA	**GND**	A18	B18	LIOB18	A14
D10	LIOA19	A19	B19	LIOB19	B13
NA	**3.3V**	A20	B20	LIOB20	A13
B8	LIOA21	A21	B21	LIOB21	B12
NA	**GND**	A22	B22	LIOB22	C18
A7	LIOA23	A23	B23	LIOB23	D17
NA	**2.5V**	A24	B24	LIOB24	C17
B7	LIOA25	A25	B25	LIOB25	D16
NA	**GND**	A26	B26	LIOB26	C16
B6	LIOA27	A27	B27	LIOB27	D15
NA	**Vin**	A28	B28	LIOB28	C15
A5	LIOA29	A29	B29	LIOB29	D14
NA	**GND**	A30	B30	LIOB30	C14
B5	LIOA31	A31	B31	LIOB31	D13
NA	**3.3V**	A32	B32	LIOB32	C13
A4	LIOA33	A33	B33	LIOB33	E13
NA	**GND**	A34	B34	LIOB34	C12
B4	LIOA35	A35	B35	LIOB35	D12
NA	**2.5V**	A36	B36	LIOB36	E12
A3	LIOA37	A37	B37	LIOB37	C9
NA	**GND**	A38	B38	LIOB38	D9
B3	LIOA39	A39	B39	LIOB39	C8
NA	**Vin**	A40	B40	LIOB40	D8

Table 14 – JX2 User I/O Connector

FPGA Pin #	I/O Connector Signal Name	JX2 Pin #		I/O Connector Signal Name	FPGA Pin #
V14	RIOA1	A1	B1	**GND**	NA
Y14	RIOA2	A2	B2	RIOB2	W18
W13	RIOA3	A3	B3	**Vin**	NA
Y18	RIOA4	A4	B4	RIOB4	W17
Y13	RIOA5	A5	B5	**GND**	NA
Y17	RIOA6	A6	B6	RIOB6	W16
V13	RIOA7	A7	B7	**3.3V**	NA
Y16	RIOA8	A8	B8	RIOB8	W15
Y12	RIOA9	A9	B9	**GND**	NA
Y15	RIOA10	A10	B10	RIOB10	W14
V12	RIOA11	A11	B11	**2.5V**	NA
AB20	RIOA12	A12	B12	RIOB12	AA20
V11	RIOA13	A13	B13	**GND**	NA
AA19	RIOA14	A14	B14	RIOB14	AA18
W11	RIOA15	A15	B15	**Vin**	NA
AB18	RIOA16	A16	B16	RIOB16	AA17
V10	RIOA17	A17	B17	**GND**	NA
AB17	RIOA18	A18	B18	RIOB18	AB16
Y10	RIOA19	A19	B19	**3.3V**	NA
AA15	RIOA20	A20	B20	RIOB20	AB15
W10	RIOA21	A21	B21	**GND**	NA
AA14	RIOA22	A22	B22	RIOB22	AB14
Y9	RIOA23	A23	B23	**2.5V**	NA
AA13	RIOA24	A24	B24	RIOB24	AB13
W9	RIOA25	A25	B25	**GND**	NA
AA12	RIOA26	A26	B26	RIOB26	AB11
Y8	RIOA27	A27	B27	**Vin**	NA
AB10	RIOA28	A28	B28	RIOB28	AA10
W8	RIOA29	A29	B29	**GND**	NA
AB9	RIOA30	A30	B30	RIOB30	AA9
Y7	RIOA31	A31	B31	**3.3V**	NA
AB8	RIOA32	A32	B32	RIOB32	AA8
W7	RIOA33	A33	B33	**GND**	NA
AA7	RIOA34	A34	B34	RIOB34	AB6
Y6	RIOA35	A35	B35	**2.5V**	NA
AA6	RIOA36	A36	B36	RIOB36	AB5
W6	RIOA37	A37	B37	**GND**	NA
AA5	RIOA38	A38	B38	RIOB38	AB4
W5	RIOA39	A39	B39	**Vin**	NA
AA4	RIOA40	A40	B40	RIOB40	AB3

4 Design Download

The Spartan-II development board supports multiple methods of configuring the Spartan-II FPGA. The JTAG port on the Spartan-II development board can be used to directly configure the Spartan-II FPGA, or to program the on-board XC18V02 ISP PROM. Once the ISP PROM is programmed, it can be used to configure the Spartan-II FPGA. The Slave Parallel/Slave Serial port on this development board can also be used to configure the Spartan-II FPGA. The following figure shows the setup for all Spartan-II FPGA configuration modes that are supported on the Spartan-II development board.

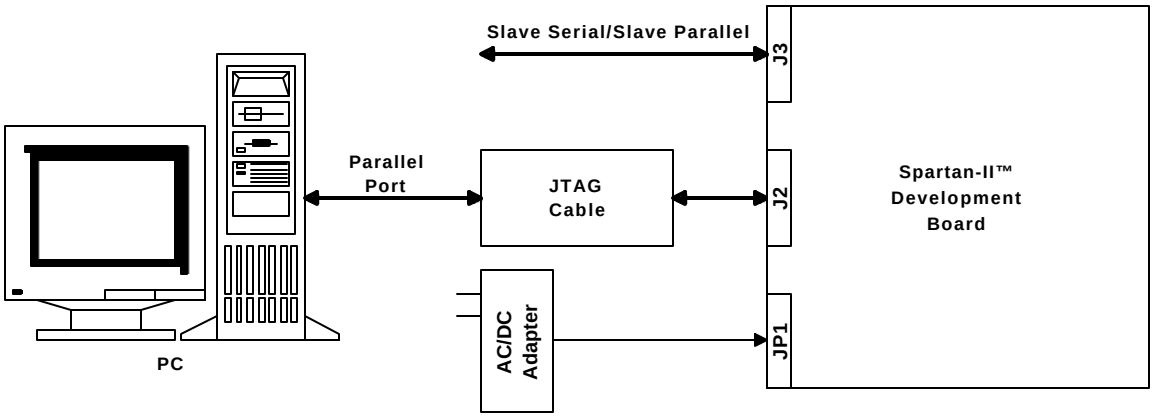


Figure 15 – Download Setup

4.1 JTAG Interface

The J2 JTAG connector on the Spartan-II development board can be used to configure the Spartan-II or to program the on-board XC18V02 ISP PROM. The Memec Design JTAG cable is connected to the Spartan-II development board via J2 at one end and to the PC parallel port at the other end.

4.1.1 Configuring the Spartan-II FPGA

When the JTAG port is used to configure the Spartan-II FPGA, the following steps must be taken:

- Using Table 13 set the Configuration Mode of the Spartan-II FPGA to JTAG Mode.
- Install the JP25 jumper if the P160 module is not present
- Install JP12 in position 2-3.
- Use the Xilinx JTAG programmer (iMPACT) utility to load the design bit file into the Spartan-II FPGA. You will need to associate the ISP PROM with either a dummy .mcs file, or a .bsd file to allow the JTAG programming software to pass data through the ISP PROM.

4.1.2 Programming the XC18V02 ISP PROM

When the JTAG port is used to program the ISP PROM, the following steps must be taken:

- Using Table 13 set the Configuration Mode of the Spartan-II FPGA to Master Serial Mode.
- Install the JP25 jumper if the P160 module is not present
- Install JP12 in position 2-3.

- Use the Xilinx JTAG programmer utility (iMPACT) to load the design mcs file into the ISP PROM. You will need to associate the FPGA with either a dummy .bit file or a .bsd file to allow the JTAG programming software to pass data through the FPGA.
- Upon programming of the 18V02 ISP PROM, the on-board PROGn push button switch (SW2) is used to initiate the Spartan-II FPGA configuration.

4.2 Slave Serial Interface

In this mode, an external source provides the configuration bit stream and the configuration clock (CCLK) to the Spartan-II FPGA. Refer to Table 13 for setting up the Configuration Mode pins.
The JP12 jumper must be installed in position 1-2 for this mode of configuration.

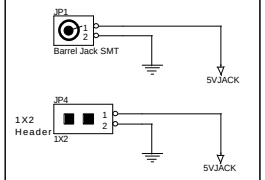
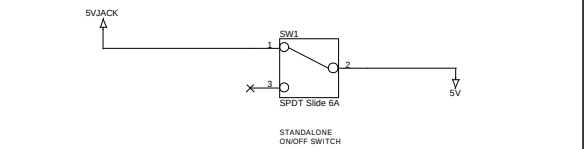
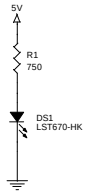
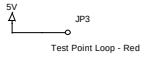
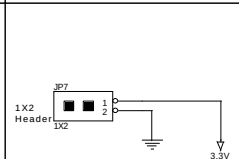
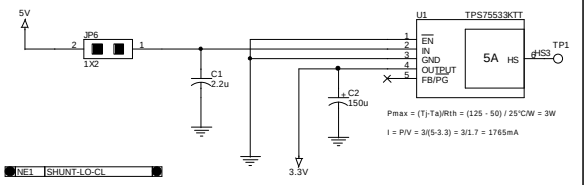
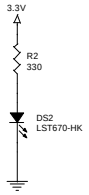
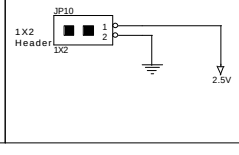
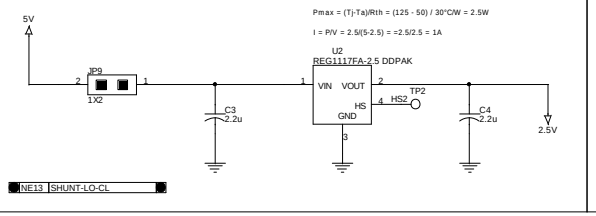
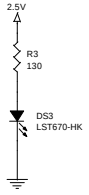
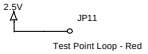
4.3 Slave Parallel

In this mode, an external source provides the configuration bit stream and the configuration clock (CCLK) to the Spartan-II FPGA. Refer to Table 13 for setting up the Configuration Mode pins.
The JP12 jumper must be installed (position 1-2) for this mode of configuration.

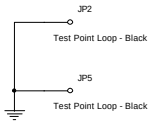
Revision History

V1.0	**Initial Release**	**4/1/02**

Appendix A - Spartan-II 200 PCI Board Schematics

VOLTAGE	INPUT JACK	REGULATION	LED	TEST LOOP
VIN (5V)				
3.3V				
2.5V				

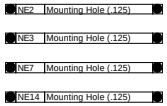
GROUND TEST LOOPS



BRACKET

RUBBER FEET

MOUNTING HOLES

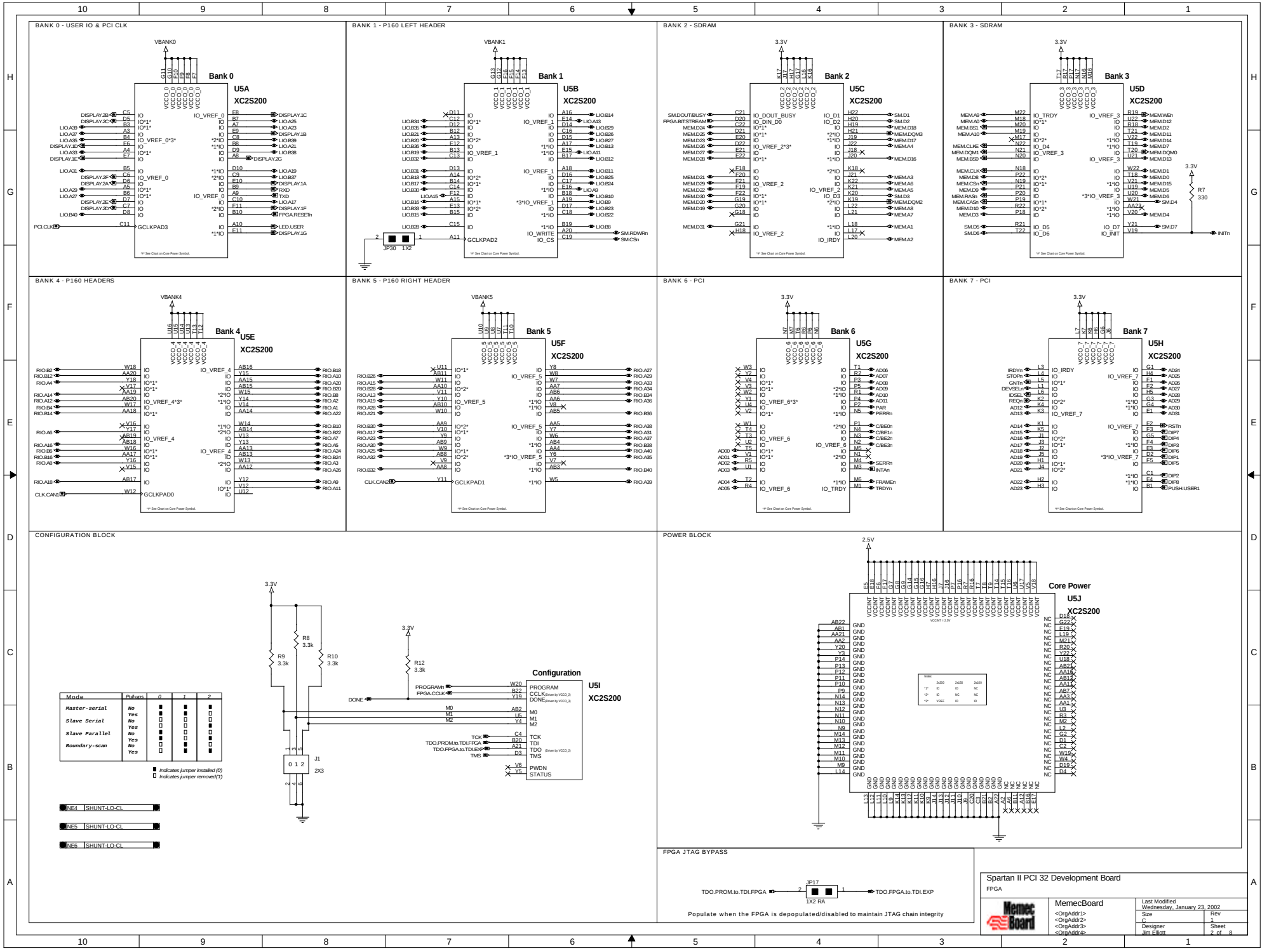


SPARTAN-II PCI : DS-BD-2S200PCI

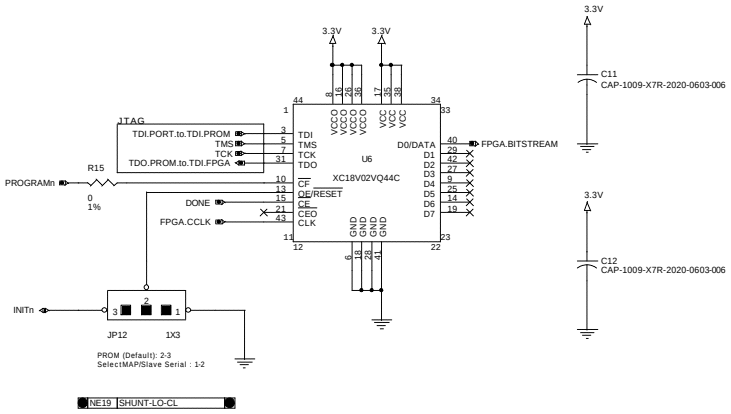
Spartan II PCI 32 Development Board

POWER

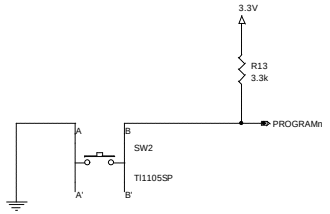
Memec Board	MemecBoard <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>	Last Modified Wednesday, January 23, 2002	
		Size C	Rev 1
		Designer Jim Elliott	Sheet 1 of 8


BANK 0 - USER IO & PCI CLK
BANK 1 - P160 LEFT HEADER
BANK 2 - SDRAM
BANK 3 - SDRAM
BANK 4 - P160 HEADERS
BANK 5 - P160 RIGHT HEADER
BANK 6 - PCI
BANK 7 - PCI
CONFIGURATION BLOCK
POWER BLOCK
FPGA JTAG BYPASS
Bank 0
Bank 1
Bank 2
Bank 3
Bank 4
Bank 5
Bank 6
Bank 7
U5A
U5B
U5C
U5D
U5E
U5F
U5G
U5H
U5I
U5J
XC2S200
Configuration
Core Power
3.3V
2.5V
JP30 1X2
JP17 1X2 RA
J1 2X3
R7 330
R8 3.3k
R9 3.3k
R10 3.3k
R12 3.3k
Mode
Master-serial
Slave Serial
Slave Parallel
Boundary-scan
Indicates jumper installed (0)
Indicates jumper removed(1)
SHUNT-LO-CL
Populate when the FPGA is depopulated/disabled to maintain JTAG chain integrity
Spartan II PCI 32 Development Board
FPGA
MemecBoard
Last Modified Wednesday, January 23, 2002
Size C
Rev 1
Designer Jim Elliott
Sheet 2 of 8

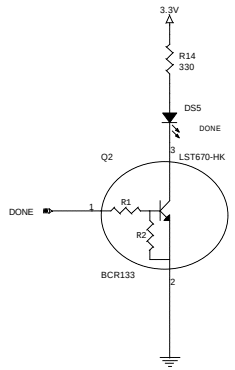
XC18 PROM



PROGRAM PUSHBUTTON



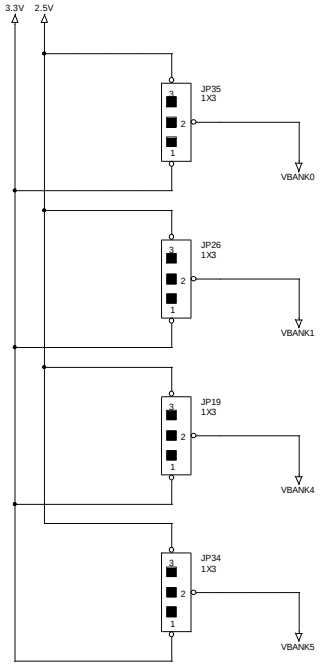
PROGRAMMING DONE LED



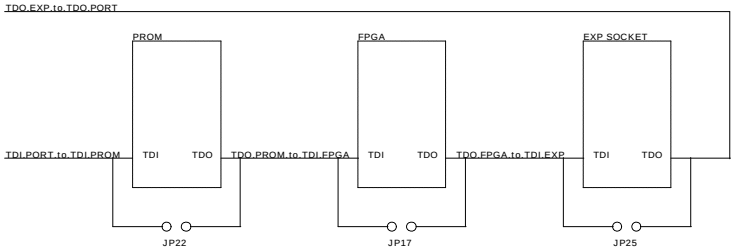
PROM JTAG BYPASS

Populate when the XC18 PROM is depopulated/disabled to maintain JTAG chain integrity

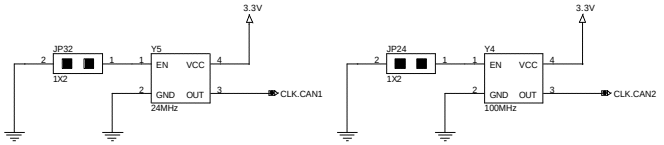
FPGA POWER SELECT

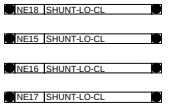


JTAG CHAIN DIAGRAM

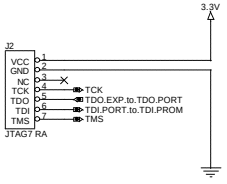


CLOCK

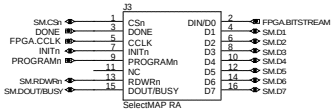




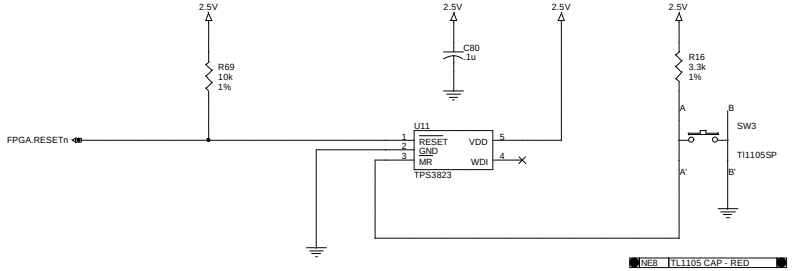
JTAG PORT



SELECTMAP PORT



FPGA RESET CIRCUIT



Spartan II PCI 32 Development Board

FPGA PERIPHERALS

MemecBoard

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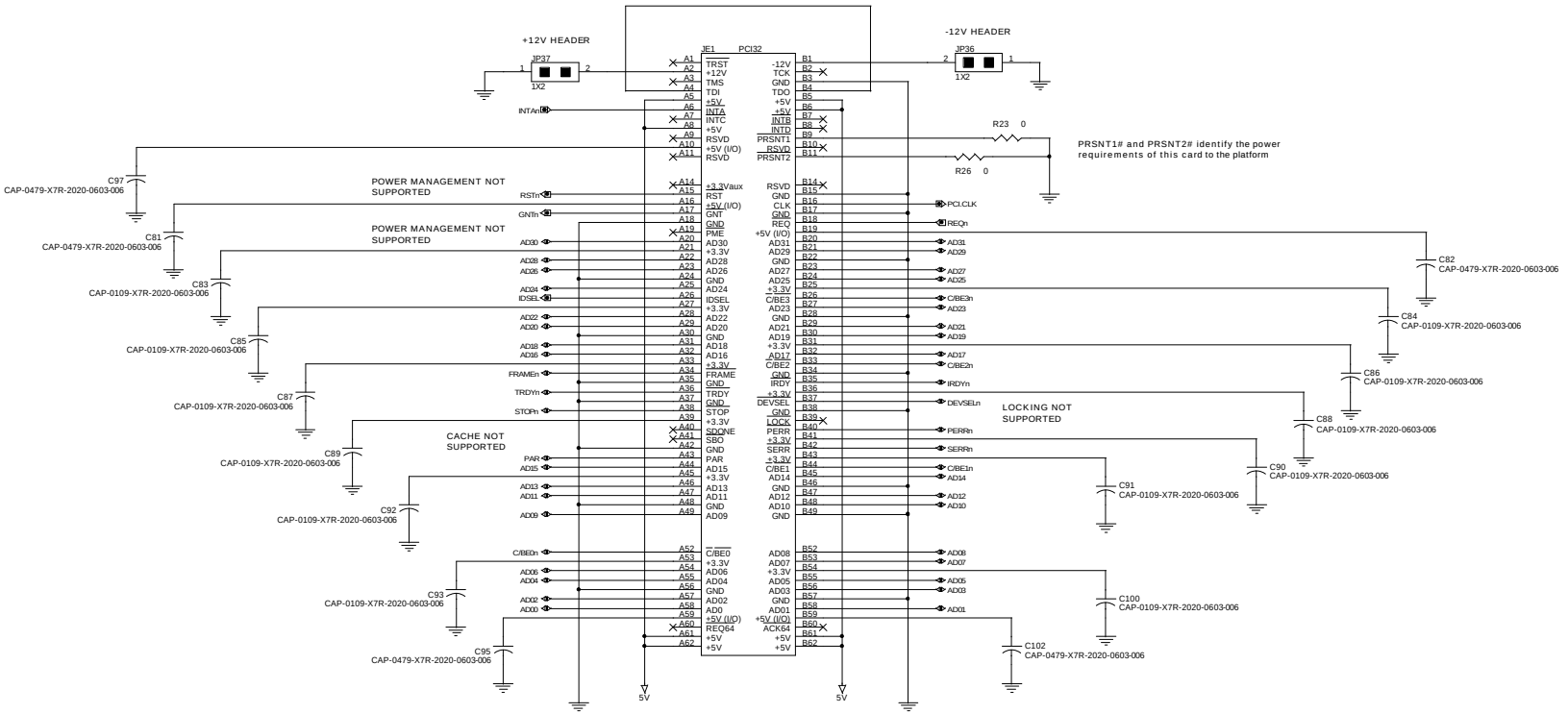
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Last Modified	Wednesday, January 23, 2002
Size	Rev
C	1
Designer	Sheet
Jim Elliott	3 of 8



Spartan II PCI 32 Development Board

PCI 32 BIT EDGE

MemecBoard

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<OrgAddr2>
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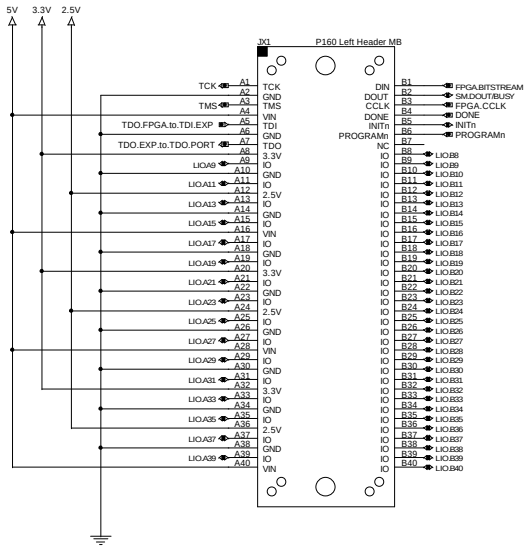
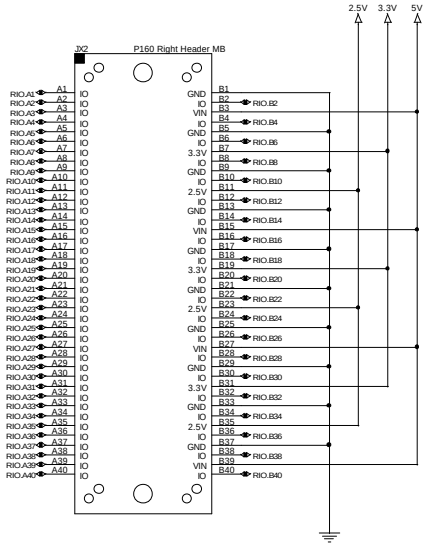
Last Modified: Wednesday, January 23, 2002

Size: C | Rev: 1

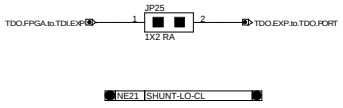
Designer: Jim Elliott | Sheet: 4 of 8

EXP SOCKET





JTAG BYPASS



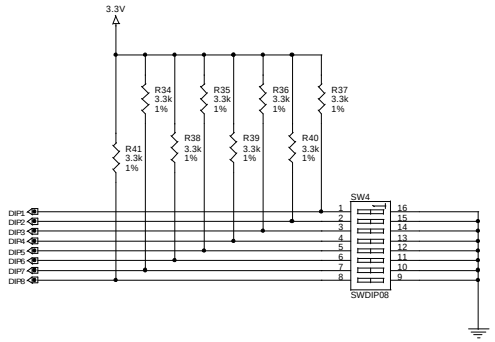
Spartan II PCI 32 Development Board

EXP SOCKET

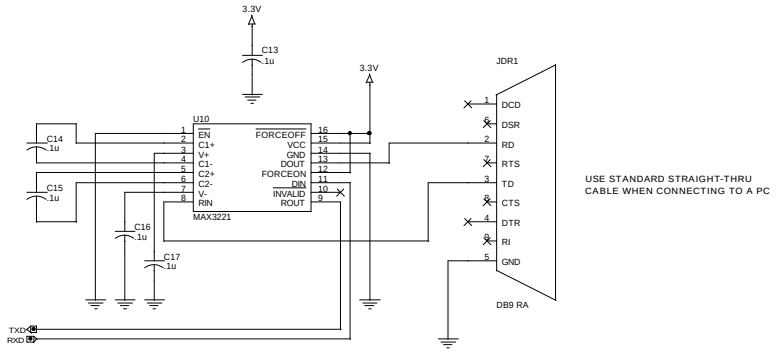
MemecBoard
Suite 540, 1212 31st Ave. NE
Calgary, Alberta
Canada
T2E 7S8

Last Modified: Wednesday, January 23, 2002
Size: C
Rev: 1
Designer: Jim Elliott
Sheet: 5 of 8

DIP SWITCH

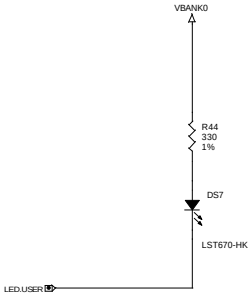


SERIAL PORT

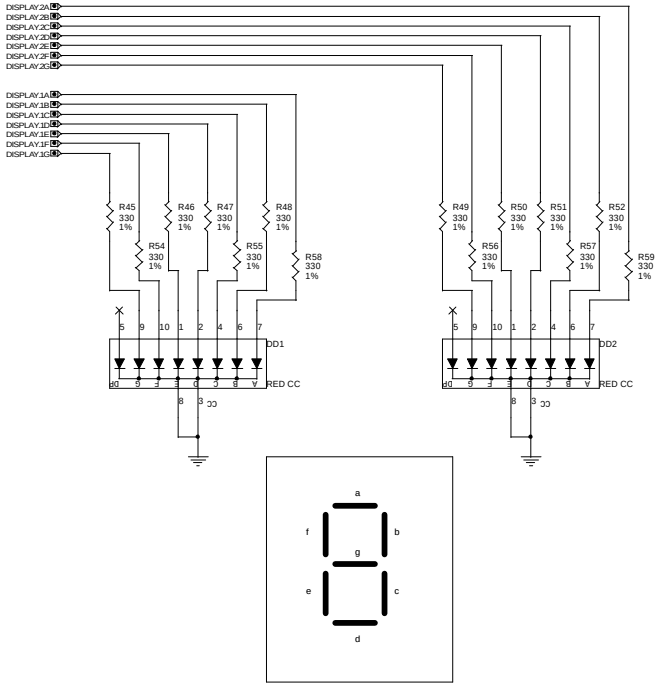


USE STANDARD STRAIGHT-THRU CABLE WHEN CONNECTING TO A PC

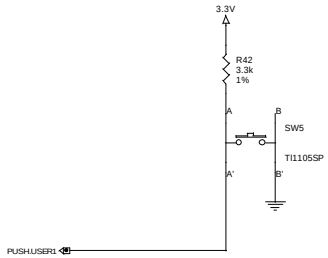
LEDs



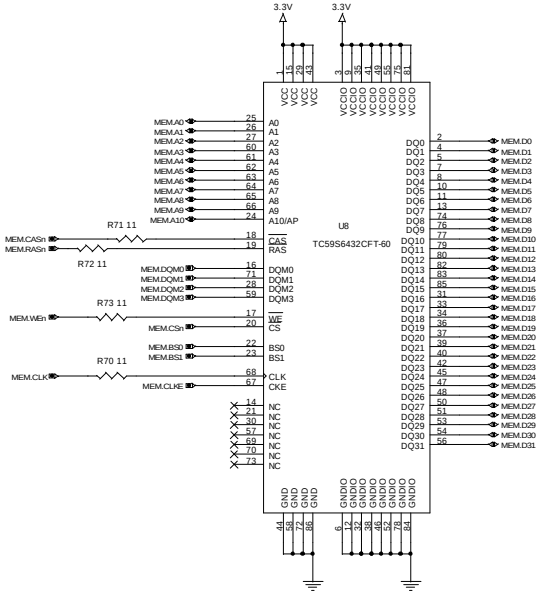
SEVEN SEGMENT DISPLAYS



PUSHBUTTONS



Spartan II PCI 32 Development Board		
USER IO		
MemecBoard Suite 540, 1212 31st Ave. NE Calgary, Alberta Canada T2E 7S8	Last Modified Wednesday, January 23, 2002 Size: C — Rev: 1 Designer: Jim Elliott — Sheet: 6 of 8	



Spartan II PCI 32 Development Board

SDRAM

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Canada
T2E 7S8

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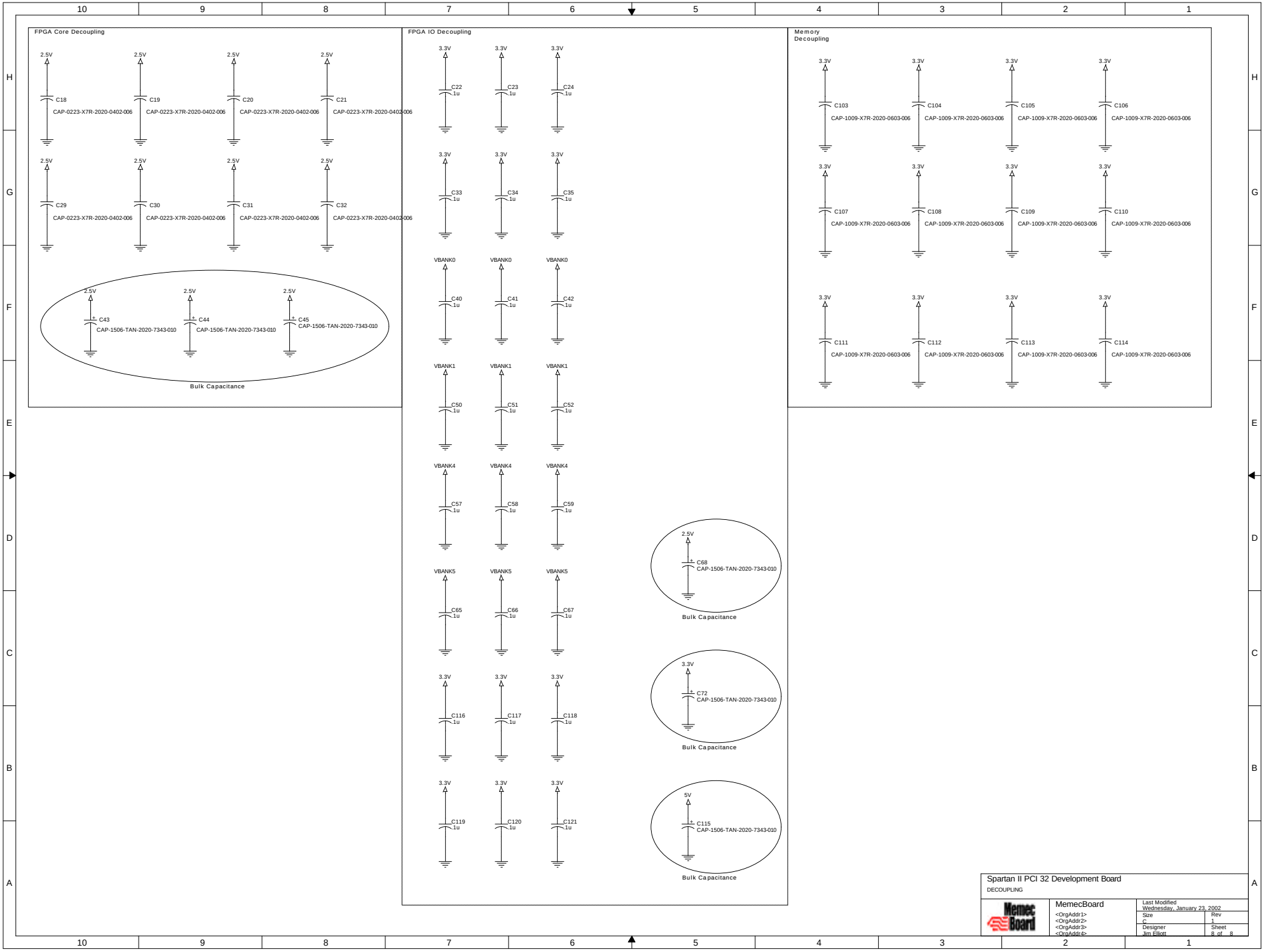
Size: C
Rev: 1
Designer: Jim Elliott
Sheet: 7 of 8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Bulk Capacitance
FPGA IO Decoupling
3.3V
C22
1u
C23
1u
C24
1u
C33
1u
C34
1u
C35
1u
VBANK0
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5V
C115
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Bulk Capacitance
Memory Decoupling
C103
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Wednesday, January 23, 2002
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Designer
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8 of 8