PCI Bus Quick Reference

by Doug Abbott

This quick reference to the PCI Bus is based on the information contained in ***PCI BUS DEMYSTIFIED*** by Doug Abbott, published by LLH Technology Publishing. To order this book in print or electronic form, visit www.LLH-Publishing.com. For more information about the PCI Bus, visit the on-line PCI bus community at www.pcibusdemystified.com.

About Doug Abbott

Doug Abbott is the founder of Intellimetrix, a New Mexico consulting firm offering PCI design and problem-solving services. His clients have included many of Silicon Valley's top computing and electronics firms. In addition to consulting, Doug has conducted many seminars and short courses about the PCI Bus and other topics (such as real-time Linux).

Notes Used In This Document

1. *Italics* indicate optional signals.
2. CLKRUN# is defined for mobile environments only and does not apply to plug-in cards.
3. Absence of a pin designation means the signal is not used in that implementation.
4. Vio is +5V in 5V signaling environments and +3.3V in 3.3V signaling environments.
5. Side B = Component Side, Side A = Solder Side.
6. System slot only.
7. "Res" = Reserved, "Bus Res" = Reserved and bussed to all slots in the segment.
8. Power Management Bus, defined by PICMG 2.9, *Compact PCI System Management Specification.*
9.  = Long Pin

    = Short Pin

PCI Signals (32-bit)

Signal Name	PCI	Compact PCI (P1)	Signal Name	PCI	Compact PCI (P1)
AD[00]	A58	D24	*DEG#*		P2-C16
AD[01]	B58	A24	DEVSEL#	B37	A16
AD[02]	A57	E23	*ENUM#*		C25
AD[03]	B56	C23	*FAL#*		P2-C15
AD[04]	A55	B23	FRAME#	A34	B15
AD[05]	B55	E22	GA[0]		P2-A22
AD[06]	A54	D22	GA[1]		P2-B22
AD[07]	B53	A22	GA[2]		P2-C22
AD[08]	B52	C21	GA[3]		P2-D22
AD[09]	A49	B21	GA[4]		P2-E22
AD[10]	B48	E20	GNT#	A17	E5
AD[11]	A47	D20	*HLTHY#*		B4
AD[12]	B47	A20	IDSEL	A26	B9
AD[13]	A46	E19	*IMB_PWR*		A4
AD[14]	B45	C19	*IMB_SCL*		B17
AD[15]	A44	B19	*IMB_SDA*		C17
AD[16]	A32	C11	INTA#	A6	A3
AD[17]	B32	B11	INTB#	B7	B3
AD[18]	A31	A11	INTC#	A7	C3
AD[19]	B30	E10	INTD#	B8	E3
AD[20]	A29	D10	*INTP*		D4
AD[21]	B29	A10	*INTS*		E4
AD[22]	A28	E9	IRDY#	B35	C15
AD[23]	B27	C9	LOCK#	B39	E16
AD[24]	A25	E8	M66EN	B49	D21
AD[25]	B24	D8	PAR	A43	D18
AD[26]	A23	A8	PERR#	B40	E17
AD[27]	B23	E7	*PME#*	A19	
AD[28]	A22	C7	PRSNT1#	B9	
AD[29]	B21	B7	PRSNT2#	B11	
AD[30]	A20	A7	*PRST#*		P2-C17
AD[31]	B20	E6	REQ#	B18	A6
BDSEL#		D15	RST#	A15	C5
C/BE[0]	A52	E21	SERR#	B42	A18
C/BE[1]	B44	E18	STOP#	A38	D16
C/BE[2]	B33	E11	SYSEN#		P2-C2
C/BE[3]	B26	A9	TRDY#	A36	E15
CLK	B16	D6	*3.3Vaux*	A14	
CLKRUN#	(2)				

PCI Signals (64-bit Extension & JTAG)

Signal Name	PCI	Compact PCI (P2)	Signal Name	PCI	Compact PCI (P2)
ACK64#	B60	P1-E24	AD[53]	B75	E8
AD[32]	A91	E14	AD[54]	A74	C8
AD[33]	B90	C14	AD[55]	B74	B8
AD[34]	A89	B14	AD[56]	A73	A8
AD[35]	B89	A14	AD[57]	B72	E7
AD[36]	A88	E13	AD[58]	A71	D7
AD[37]	B87	D13	AD[59]	B71	A7
AD[38]	A86	A13	AD[60]	A70	E6
AD[39]	B86	E12	AD[61]	B69	C6
AD[40]	A85	C12	AD[62]	A68	B6
AD[41]	B84	B12	AD[63]	B68	A6
AD[42]	A83	A12	C/BE[4]	B66	D5
AD[43]	B83	E11	C/BE[5]	A65	A5
AD[44]	A82	D11	C/BE[6]	B65	E4
AD[45]	B81	A11	C/BE[7]	A64	C4
AD[46]	A80	E10	PAR64	A67	E5
AD[47]	B80	C10	REQ64#	A60	P1-B25
AD[48]	A79	B10	TCK	B2	P1-A2
AD[49]	B78	A10	TDI	A4	P1-E2
AD[50]	A77	E9	TDO	B4	P1-D2
AD[51]	B77	D9	TMS	A3	P1-C2
AD[52]	A76	A9	TRST#	A1	P1-C1

PCI Connector

Pin	Side B[5]	Side A	Pin	Side B	Side A
1	-12V	TRST#	49	M66EN	AD[09]
2	TCK	+12V	50	3.3V: Gnd	
3	Gnd	TMS	51	5V: Keyway	
4	TDO	TDI	52	AD[08]	C/BE[0]
5	+5V	+5V	53	AD[07]	+3.3V
6	+5V	INTA#	54	+3.3V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5V	56	AD[03]	Gnd
9	PRSNT1#	Reserved	57	Gnd	AD[02]
10	Reserved	+Vio [4]	58	AD[01]	AD[00]
11	PRSNT2#	Reserved	59	+Vio [4]	+Vio [4]
12	3.3V: Keyway		60	ACK64#	REQ64#
13	5V: Gnd		61	+5V	+5V
14	Reserved	3.3Vaux	62	+5V	+5V
15	Gnd	RST#	KEYWAY, 64 Bit Spacer		
16	CLK	+Vio [4]			
17	Gnd	GNT#	63	Reserved	Gnd
18	REQ#	Gnd	64	Gnd	C/BE[7]
19	+Vio [4]	PME#	65	C/BE[6]	C/BE[5]
20	AD[31]	AD[30]	66	C/BE[4]	+Vio [4]
21	AD[29]	+3.3V	67	Gnd	PAR64
22	Gnd	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Gnd
24	AD[25]	Gnd	70	+Vio	AD[60]
25	+3.3V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]	IDSEL	72	AD[57]	Gnd
27	AD[23]	+3.3V	73	Gnd	AD[56]
28	Gnd	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+Vio [4])
30	AD[19]	Gnd	76	Gnd	AD[52]
31	+3.3V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Gnd
33	C/BE[2]	+3.3V	79	+Vio [4]	AD[48]
34	Gnd	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Gnd	81	AD[45]	Gnd
36	+3.3V	TRDY#	82	Gnd	AD[44]
37	DEVSEL#	Gnd	83	AD[43]	AD[42]
38	Gnd	STOP#	84	AD[41]	+Vio [4]
39	LOCK#	+3.3V	85	Gnd	AD[40]
40	PERR#	Reserved	86	AD[39]	AD[38]
41	+3.3V	Reserved	87	AD[37]	Gnd
42	SERR#	Gnd	88	+Vio [4]	AD[36]
43	+3.3V	PAR	89	AD[35]	AD[34]
44	C/BE[1]	AD[15]	90	AD[33]	Gnd
45	AD[14]	+3.3V	91	Gnd	AD[32]
46	Gnd	AD[13]	92	Reserved	Reserved
47	AD[12]	AD[11]	93	Reserved	Gnd
48	AD[10]	Gnd	94	Gnd	Reserved

Compact PCI Connectors

P2

Pin	A	B	C	D	E
22	GA[4]	GA[3]	GA[2]	GA[1]	GA[0]
21	CLK6 (6)	Gnd	Res (7)	Res	Res
20	CLK5 (6)	Gnd	Res	Gnd	Res
19	Gnd	Gnd	Res	Res	Res
18	Bus Res	Bus Res	Bus Res	Gnd	Bus Res
17	Bus Res	Gnd	PRST#	REQ6# (6)	GNT6# (6)
16	Bus Res	Bus Res	DEG#	Gnd	Bus Res
15	Bus Res	Gnd	FAL#	REQ5# (6)	GNT5# (6)
14	AD[35]	AD[34]	AD[33]	Gnd	AD[32]
13	AD[38]	Gnd	+Vio (4)	AD[37]	AD[36]
12	AD[42]	AD[41]	AD[40]	Gnd	AD[39]
11	AD[45]	Gnd	+Vio (4)	AD[44]	AD[43]
10	AD[49]	AD[48]	AD[47]	Gnd	AD[46]
9	AD[52]	Gnd	+Vio (4)	AD[51]	AD[50]
8	AD[56]	AD[55]	AD[54]	Gnd	AD[53]
7	AD[59]	Gnd	+Vio (4)	AD[58]	AD[57]
6	AD[63]	AD[62]	AD[61]	Gnd	AD[60]
5	C/BE[5]	Gnd	+Vio (4)	C/BE[4]	PAR64
4	+Vio (4)	Bus Res	C/BE[7]	Gnd	C/BE[6]
3	CLK4 (6)	Gnd	GNT3# (6)	REQ4# (6)	GNT4# (6)
2	CLK2 (6)	CLK3 (6)	SYSEN#	GNT2# (6)	REQ3# (6)
1	CLK1 (6)	Gnd	REQ1# (6)	GNT1# (6)	REQ2# (6)

P1

Pin	A	B	C	D	E
25	+5V	REQ64#	ENUM#	+3.3V	+5V
24	AD[01]	+5V	+Vio (4)	AD[00]	ACK64#
23	+3.3V	AD[04]	AD[03]	+5V (9)	AD[02]
22	AD[07]	Gnd	+3.3V	AD[06]	AD[05]
21	+3.3V	AD[09]	AD[08]	M66EN	C/BE[0]
20	AD[12]	Gnd	+Vio (4)	AD[11]	AD[10]
19	+3.3V	AD[15]	AD[14]	Gnd	AD[13]
18	SERR#	Gnd	+3.3V	PAR	C/BE[1]
17	+3.3V	SCL(8)	SDA(8)	Gnd	PERR#
16	DEVSEL#	Gnd	+Vio	STOP#	LOCK#
15	+3.3V	FRAME#	IRDY#	BDSEL#	TRDY#
		14 – 12	KEYWAY		
11	AD[18]	AD[17]	AD[16]	Gnd	C/BE[2]
10	AD[21]	Gnd	+3.3V	AD[20]	AD[19]
9	C/BE[3]	IDSEL (9)	AD[23]	Gnd	AD[22]
8	AD[26]	Gnd	+Vio	AD[25]	AD[24]
7	AD[30]	AD[29]	AD[28]	Gnd	AD[27]
6	REQ#	Gnd	+3.3V	CLK	AD[31]
5	Bus Res	Bus Res	RST#	Gnd	GNT#
4	PWR(8)	HLTHY#	+Vio (4)	INTP	INTS
3	INTA#	INTB#	INTC#	+5V	INTD#
2	TCK	+5V	TMS	TDO	TDI
1	+5V	-12V	TRST#	+12V	+5V

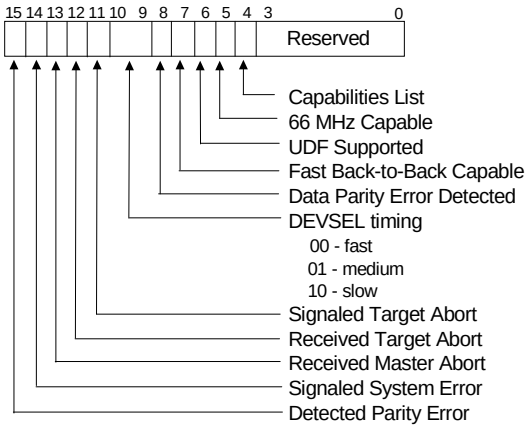
Bus Commands

C/BE					Command
3	**2**	**1**	**0**	**Hex**	
0	0	0	0	0	Interrupt Acknowledge
0	0	0	1	1	Special Cycle
0	0	1	0	2	I/O Read
0	0	1	1	3	I/O Write
0	1	0	0	4	Reserved
0	1	0	1	5	Reserved
0	1	1	0	6	Memory Read
0	1	1	1	7	Memory Write
1	0	0	0	8	Reserved
1	0	0	1	9	Reserved
1	0	1	0	A	Configuration Read
1	0	1	1	B	Configuration Write
1	1	0	0	C	Memory Read Multiple
1	1	0	1	D	Dual Address Cycle
1	1	1	0	E	Memory Read Line
1	1	1	1	F	Memory Write & Invalidate

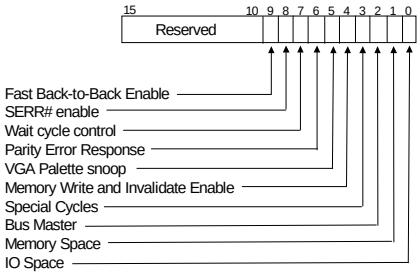
Bus State

FRAME#	DEVSEL#	IRDY#	TRDY#	STOP#	Bus State
1	1	1	1	1	Idle
0	1	1	1	1	Address Phase (1 clock)
0	1	X	1	1	Master Abort (after 4 clock cycles)
0	0	X	X	1	Target Selected
0	0	X	1	0	Target Retry (no data transfer)
0	0	0	0	1	Data Transfer
0	0	1	X	1	Initiator Delay
0	0	X	1	1	Target Delay
0	0	X	X	0	Target Disconnect (data has transferred)
1	0	X	X	1	Initiator Termination (last data transfer)
0	1	X	1	0	Target Abort (data may have transferred)
X	1	X	0	X	Invalid. Can't assert TRDY without DEVSEL

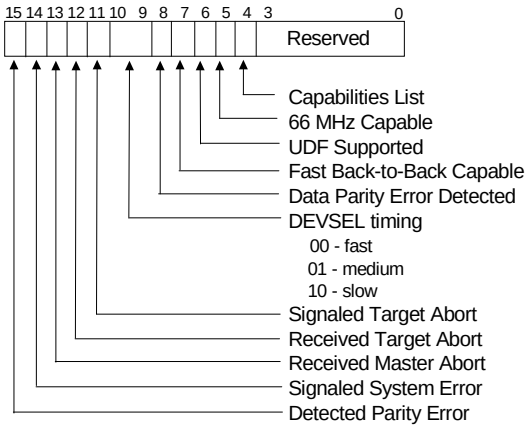
Configuration Header—Type 0



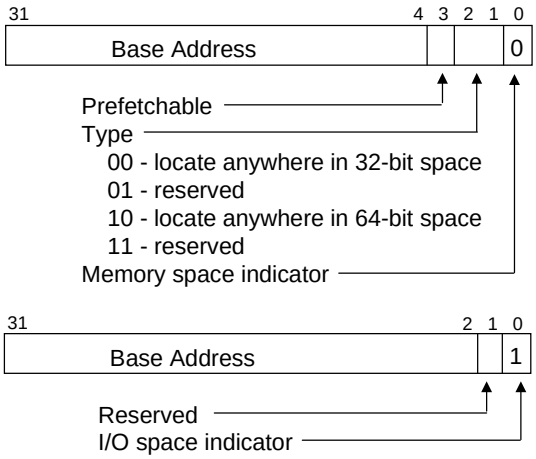
Command Register



Status Register



Base Address Registers



Class Codes

Subclass (hex)
Programming Interface (hex)

Class 00 Device predates class code definitions
- 00 Non-VGA devices
- 01 VGA devices

Class 01 Mass storage controllers
- 00 SCSI controller
- 01 IDE controller
  - xx See Note 1
- 02 Floppy disk controller
- 03 IPI bus controller
- 04 RAID controller

Class 02 Network controllers
- 00 Ethernet
- 01 Token Ring
- 02 FDDI
- 03 ATM
- 04 ISDN

Class 03 Display controllers
- 00 VGA/8514
  - 01 VGA-compatible
  - 02 8514-compatible
- 01 XGA
- 02 3-D controller

Class 04 Multimedia devices
- 00 Video
- 01 Audio
- 02 Computer telephony

Class 05 Memory controllers
- 00 RAM
- 01 Flash

Class 06 Bridge devices
- 00 Host bridge
- 01 ISA bridge
- 02 EISA bridge
- 03 MCA bridge
- 04 PCI to PCI bridge
  - 00 PCI to PCI bridge
  - 01 Supports subtractive decode
- 05 PCMCIA bridge
- 06 NuBus bridge
- 07 Cardbus bridge
- 08 RACEway bridge

Notes

1. IDE Programming interface
   - Bit 0 Operating mode (primary)
   - Bit 1 Programmable indicator (primary)
   - Bit 2 Operating mode (secondary)
   - Bit 3 Programmable indicator (secondary)
   - Bit 7 Master IDE device

Class 07 Simple communication controllers
- 00
  - 00 Generic XT-compatible serial controller
  - 01 16450-compatible serial controller
  - 02 16550-compatible serial controller
  - 03 16650-compatible serial controller
  - 04 16750-compatible serial controller
  - 05 16850-compatible serial controller
  - 06 16950-compatible serial controller
- 01
  - 00 Parallel Port
  - 01 Bi-directional parallel port
  - 02 ECP 1.X compliant parallel port
  - 03 IEEE 1284 controller
  - FE IEEE 1284 target device
- 02 Multiport serial controller
- 03
  - 00 Generic modem
  - 01 Hayes compatible, 16450 interface (2)
  - 02 Hayes compatible, 16550 interface (2)
  - 03 Hayes compatible, 16650 interface (2)
  - 04 Hayes compatible, 16750 interface (2)

Class 08 Generic system peripherals
- 00 Interrupt controllers
  - 00 Generic 8259
  - 01 ISA PIC
  - 02 EISA PIC
  - 03 I/O APIC (3)
- 01 DMA controllers
  - 00 Generic 8237
  - 01 ISA DMA
  - 02 EISA DMA
- 02 Timers
  - 00 Generic 8254
  - 01 ISA system timer
  - 02 EISA system timer (two timers)
- 03 Real-time clock
  - 00 Generic RTC
  - 01 ISA RTC
- 04 Generic PCI Hot-Plug controller

Class 09 Input devices
- 00 Keyboard controller
- 01 Digitizer (pen)
- 02 Mouse controller
- 03 Scanner controller
- 04 Gameport
  - 00 Generic
  - 02 See note 4

Class 0A Generic docking station

Class 0B Processors
- 00 386
- 01 486
- 02 Pentium
- 10 Alpha
- 20 Power PC
- 30 MIPS
- 40 Co-processor

Class 0C Serial bus controllers
- 00 IEEE 1394
  - 00 Firewire
  - 10 Open HCI specification
- 01 ACCESS.bus
- 02 SSA
- 03 USB
  - 00 Universal Host Controller specification
  - 10 Open HCI specification
  - 80 No specific programming interface
  - FE USB device, not controller
- 04 Fibre Channel
- 05 System Management Bus

Class 0D Wireless controllers
- 00 iRDA controller
- 01 Consumer IR controller
- 10 RF controller

Class 0E Intelligent I/O controllers
- 00
  - xx I2O Architecture Specification 1.0
  - 00 Message FIFO at offset 40h

Class 0F Satellite communication controllers
- 00 TV
- 01 Audio
- 02 Voice
- 03 Data

Class 10 Encryption/decryption
- 00 Network & computing en/decryption
- 10 Entertainment en/decryption

Class 11 Data acquisition & signal processing
- 00 DPIO modules

Notes

2. First BAR (10h) maps appropriate compatible register set. Registers can be either memory or I/O mapped.
3. First BAR (10h) requests minimum 32 bytes non-prefetchable space. Base+0 = I/O Select, Base+10h = I/O Window. See Intel *82420/82430 PCIset EISA Bridge Databook* (#290483-003) for more details.
4. "Legacy" game port. Byte at offset 01h aliases to byte at offset 00h.
5. For all classes except 00, subclass 80h means "other."