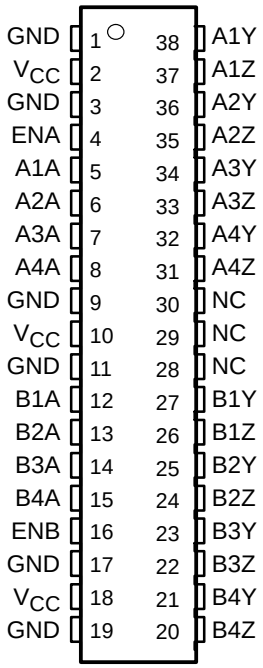
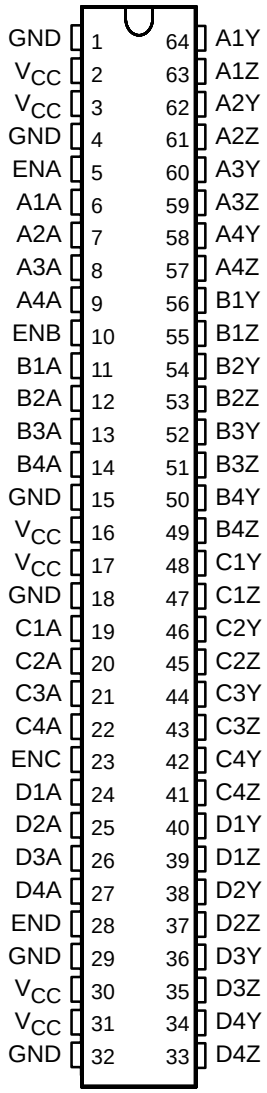
- **Four (’391), Eight (’389) or Sixteen (’387) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Designed for Signaling Rates† up to 630 Mbps With Very Low Radiation (EMI)**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Propagation Delay Times Less Than 2.9 ns**
- **Output Skew Is Less Than 150 ps**
- **Part-to-Part Skew Is Less Than 1.5 ns**
- **35-mW Total Power Dissipation in Each Driver Operating at 200 MHz**
- **Driver Is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **SN65’ Version Bus-Pin ESD Protection Exceeds 15 kV**
- **Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch**
- **Low-Voltage TTL (LVTTL) Logic Inputs Are 5-V Tolerant**

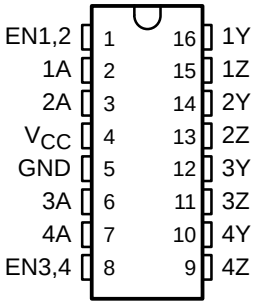
’LVDS389
DBT PACKAGE
(TOP VIEW)



’LVDS387
DGG PACKAGE
(TOP VIEW)



’LVDS391
D OR PW PACKAGE
(TOP VIEW)



description

This family of four, eight, and sixteen differential line drivers implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the sixteen current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of this device and signaling technique is for point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media can be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with the companion 16- or 8-channel receivers, the SN65LVDS386 or SN65LVDS388, over 300 million data transfers per second in single-edge clocked systems are possible with very little power. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

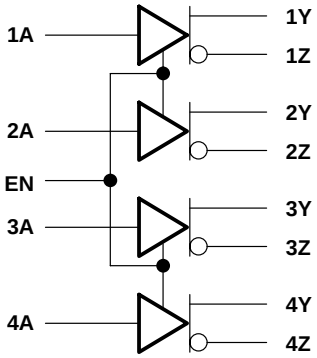
† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

description (continued)

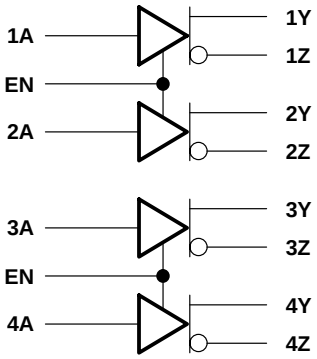
When disabled, the driver outputs are high impedance. Each driver input (A) and enable (EN) have an internal pulldown that will drive the input to a low level when open circuited.

The SN65LVDS387, SN65LVDS389, and SN65LVDS391 are characterized for operation from –40°C to 85°C. The SN75LVDS387, SN75LVDS389, and SN75LVDS391 are characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



(1/4 of ’LVDS387 or 1/2 of ’LVDS389 shown)



(’LVDS391 shown)

AVAILABLE OPTIONS

PART NUMBER†	TEMPERATURE RANGE	NO. OF DRIVERS	BUS-PIN ESD
SN65LVDS387DGG	–40°C to 85°C	16	15 kV
SN75LVDS387DGG	0°C to 70°C	16	4 kV
SN65LVDS389DBT	–40°C to 85°C	8	15 kV
SN75LVDS389DBT	0°C to 70°C	8	4 kV
SN65LVDS391D	–40°C to 85°C	4	15 kV
SN75LVDS391D	0°C to 70°C	4	4 kV
SN65LVDS391PW	–40°C to 85°C	4	15 kV
SN75LVDS391PW	0°C to 70°C	4	4 kV

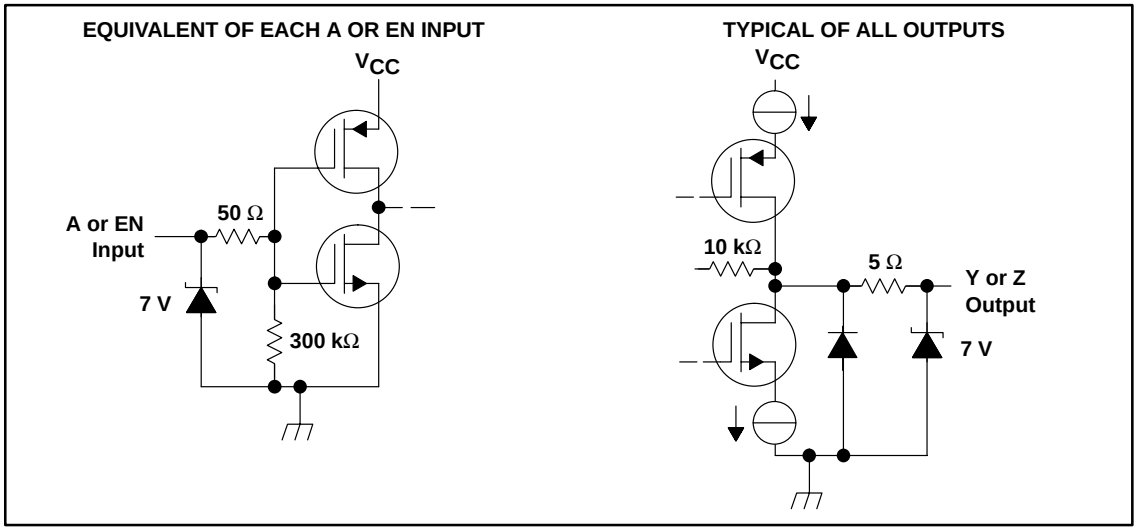
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., SN65LVDS387DGGR).

DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS	
A	EN	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
OPEN	H	L	H

H = high-level, L = low-level, X = irrelevant,
Z = high-impedance (off)

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4 V
Input voltage range: Inputs . . . . . –0.5 V to 6 V
Y or Z . . . . . –0.5 V to 4 V
Electrostatic discharge: SN65' (Y, Z, and GND) . . . . . Class 3, A:15 kV, B: 500 V
SN75' (Y, Z, and GND) . . . . . Class 3, A:4 kV, B: 400 V
Continuous power dissipation . . . . . (see Dissipation Rating Table)
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DBT	1071 mW	8.5 mW/°C	688 mW	556 mW
DGG	2094 mW	16.7 mW/°C	1342 mW	1089 mW
PW	774 mW	6.2 mW/°C	496 mW	402 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	SN75'	0		70	°C
	SN65'	–40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 1 and Figure 2		247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			−50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			−50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{CC}	Supply current	'LVDS387	Enabled, R_L = 100 Ω, V_{IN} = 0.8 V or 2 V		85	95	mA
		'LVDS389			50	70	
		'LVDS391			20	26	
		'LVDS387	Disabled, V_{IN} = 0 V or V_{CC}		0.5	1.5	
		'LVDS389			0.5	1.5	
		'LVDS391			0.5	1.3	
I_{IH}	High-level input current	V_{IH} = 2 V			3	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			2	10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V				±24	mA
		V_{OD} = 0 V				±12	mA
I_{OZ}	High-impedance output current	V_O = 0 V or V_{CC}				±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V				±1	µA
C_{IN}	Input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V			5		pF
C_O	Output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled			9.4		pF

† All typical values are at 25°C and with a 3.3-V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 4	0.9	1.7	2.9	ns
t_{PHL}	Propagation delay time, high-to-low-level output		0.9	1.6	2.9	ns
t_r	Differential output signal rise time		0.4	0.8	1	ns
t_f	Differential output signal fall time		0.4	0.8	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			150	500	ps
$t_{sk(o)}$	Output skew‡			80	150	ps
$t_{sk(pp)}$	Part-to-part skew§				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		6.4	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			5.9	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.5	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4.5	15	ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
§ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.

PARAMETER MEASUREMENT INFORMATION

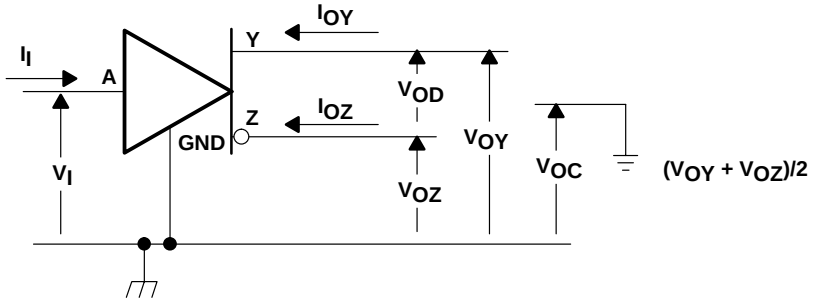


Figure 1. Voltage and Current Definitions

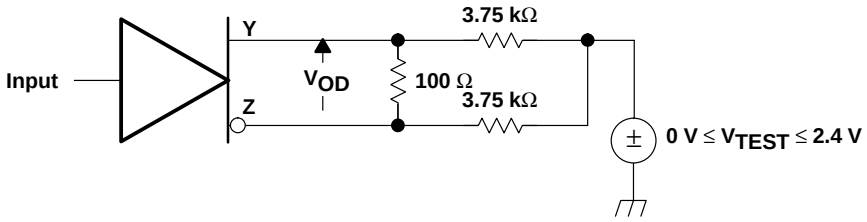
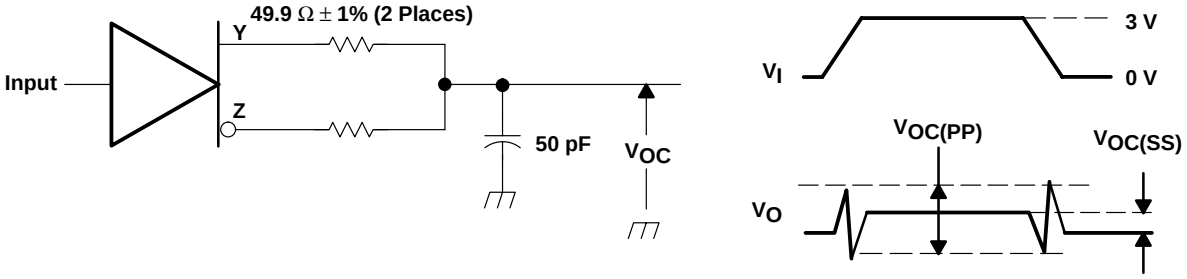
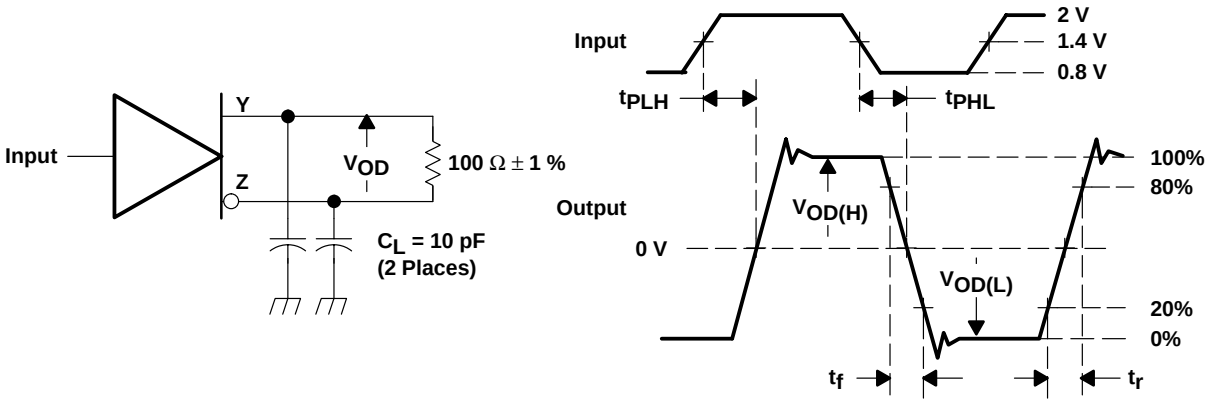


Figure 2. VOD Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

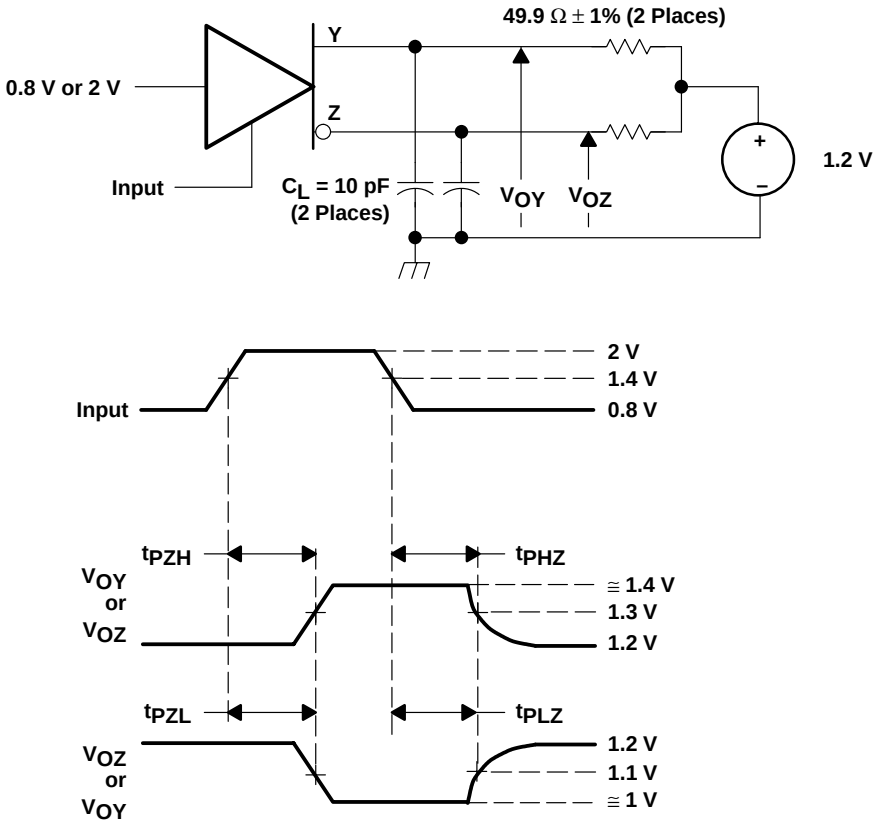
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTICS

**'LVDS391
SUPPLY CURRENT (RMS)
vs
SWITCHING FREQUENCY**

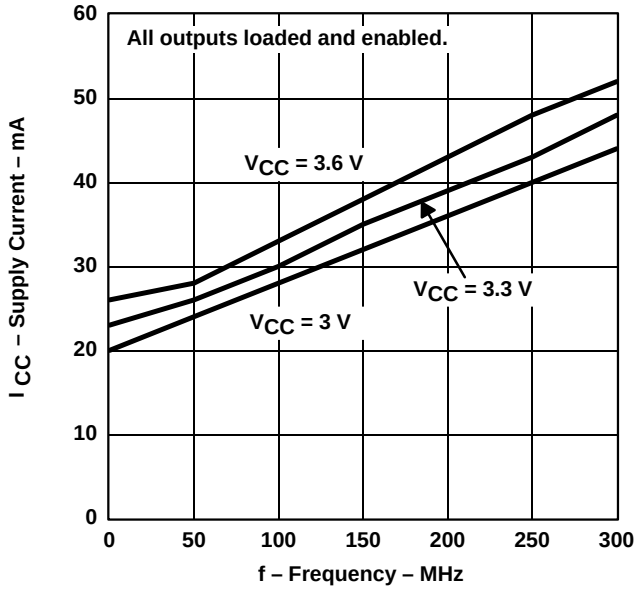


Figure 6

**'LVDS387
SUPPLY CURRENT (RMS)
vs
SWITCHING FREQUENCY**

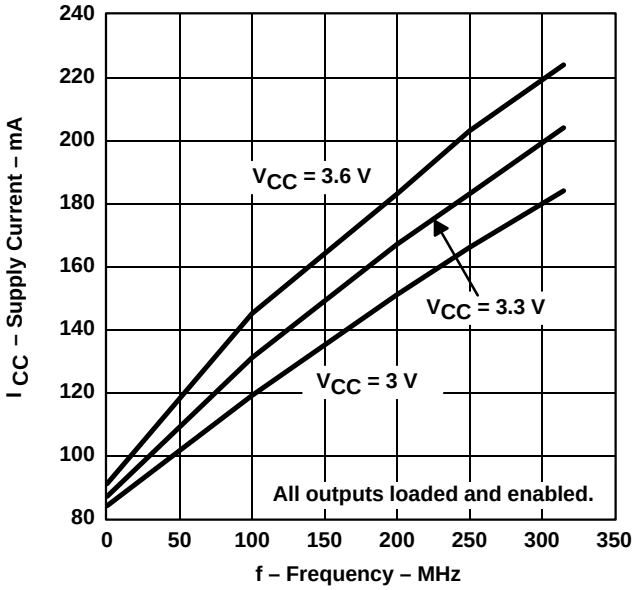


Figure 7

**'LVDS389
SUPPLY CURRENT (RMS)
vs
SWITCHING FREQUENCY**

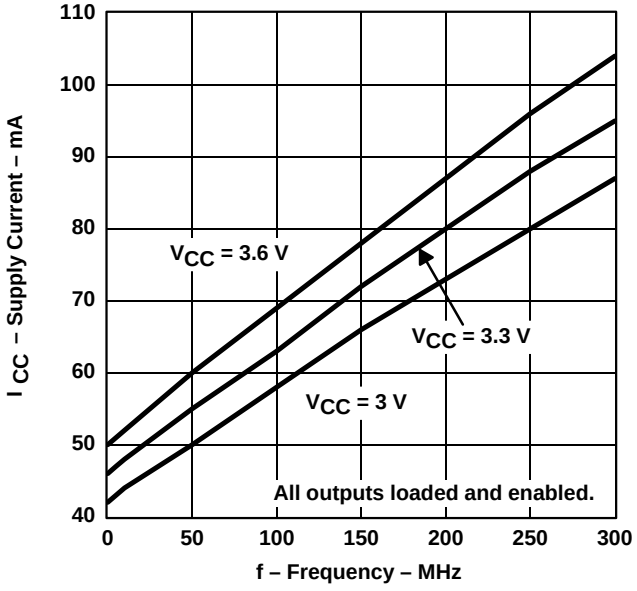


Figure 8

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

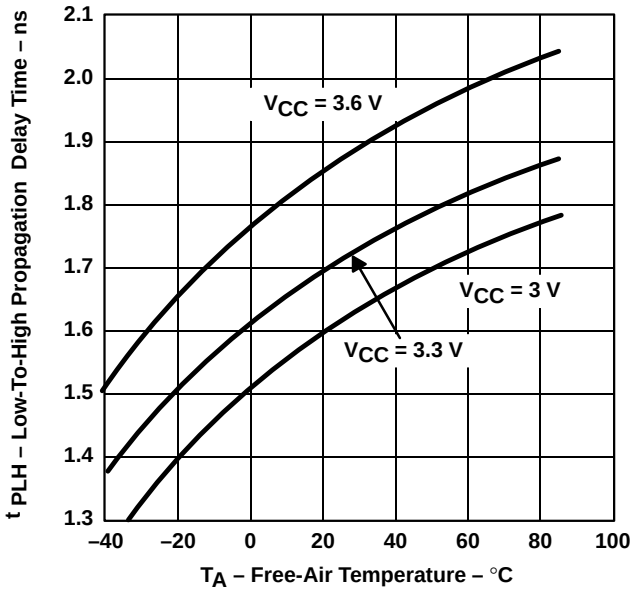


Figure 9

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

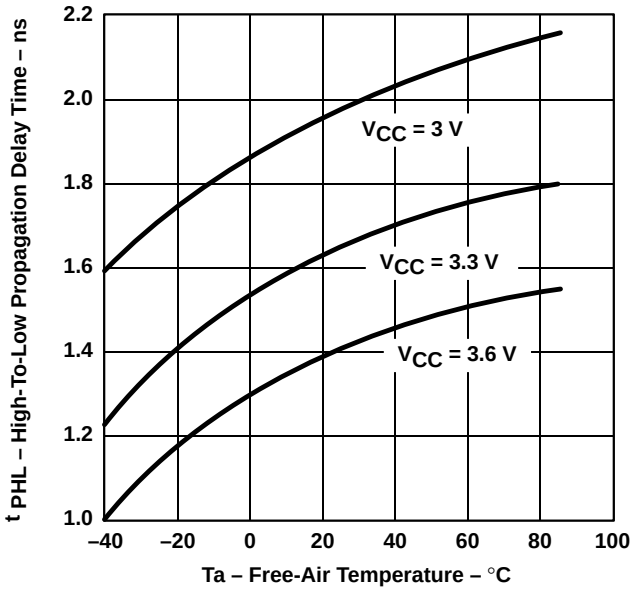


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

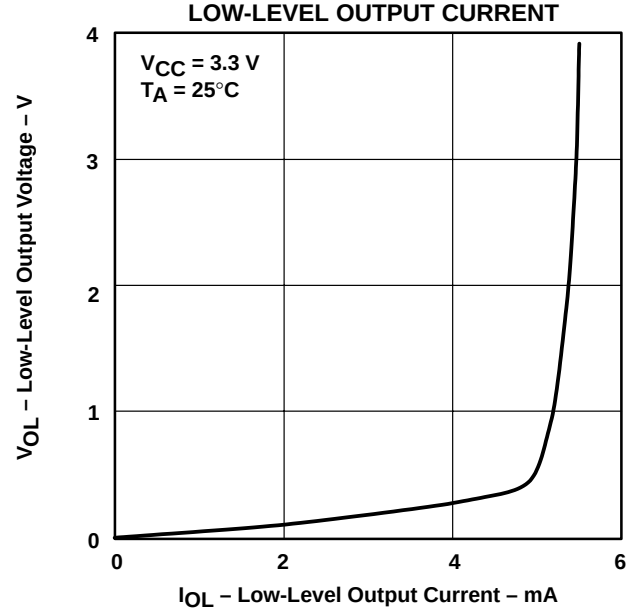


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

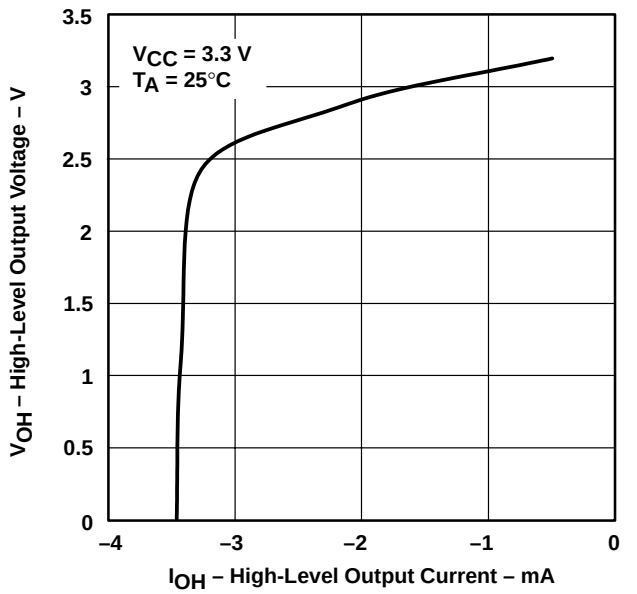
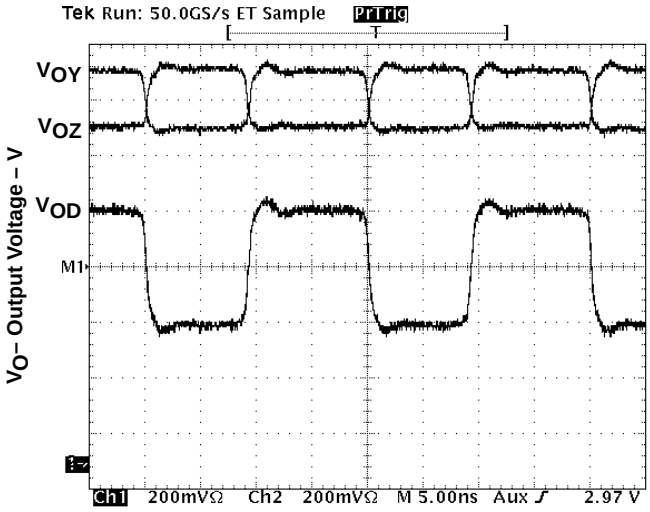


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
TIME



t – Time – ns

Figure 13

APPLICATION INFORMATION

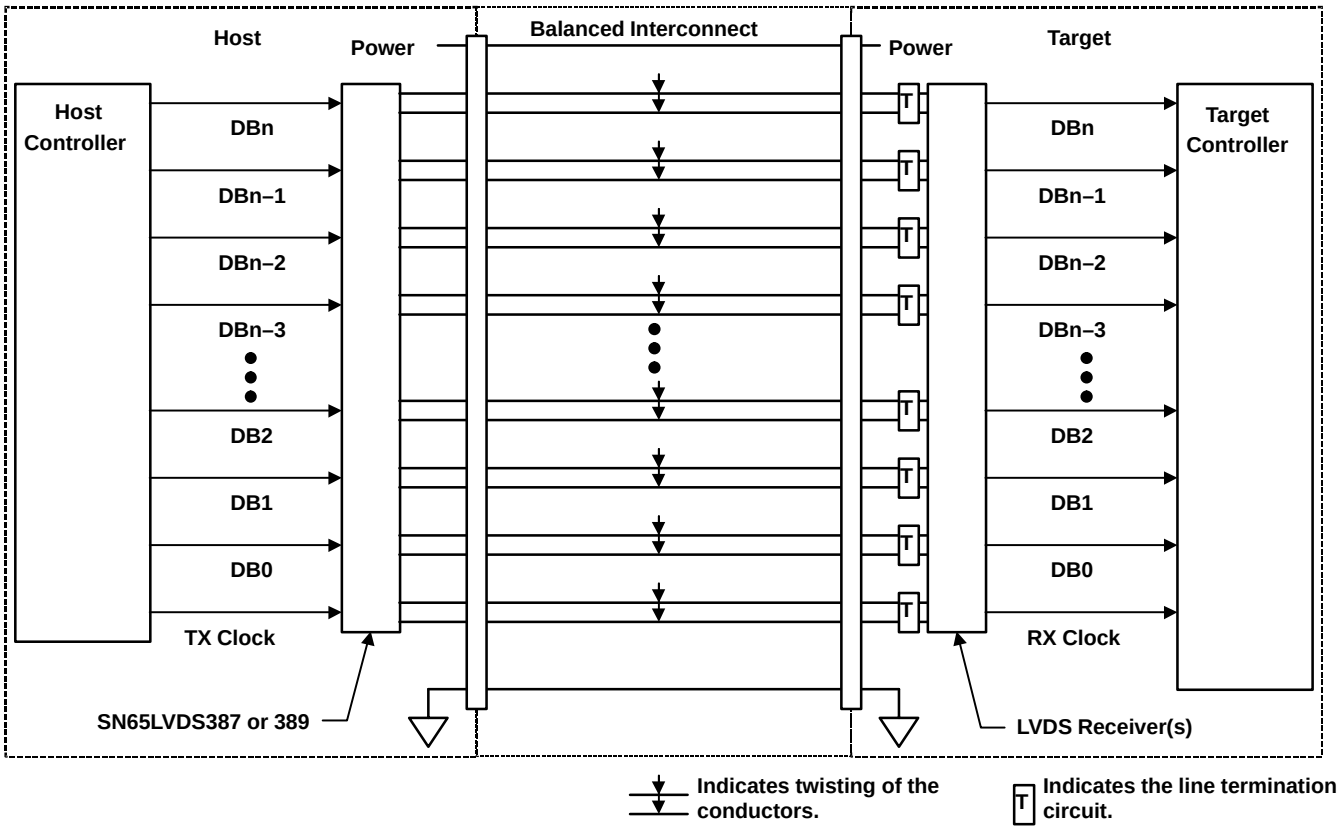


Figure 14. Typical Application Schematic

Signaling Rate vs Distance

The ultimate data transfer rate over a given cable or trace length involves many variables. Starting with the capabilities of this LVDS driver to reproduce a data pulse as short as 1.6 ns (a 630 Mbps signaling rate) with less than 500 ps of pulse distortion, any degradation of this pulse by the transmission media will necessarily reduce the timing margin at the receiving end of the data link.

The timing uncertainty induced by the transmission media is commonly referred to as jitter and comes from numerous sources. The characteristics of a particular transmission media can be quantified by using an eyepattern measurement such as shown in Figure 12, which shows about 340 ps of jitter or 20% of the data pulse width.

APPLICATION INFORMATION

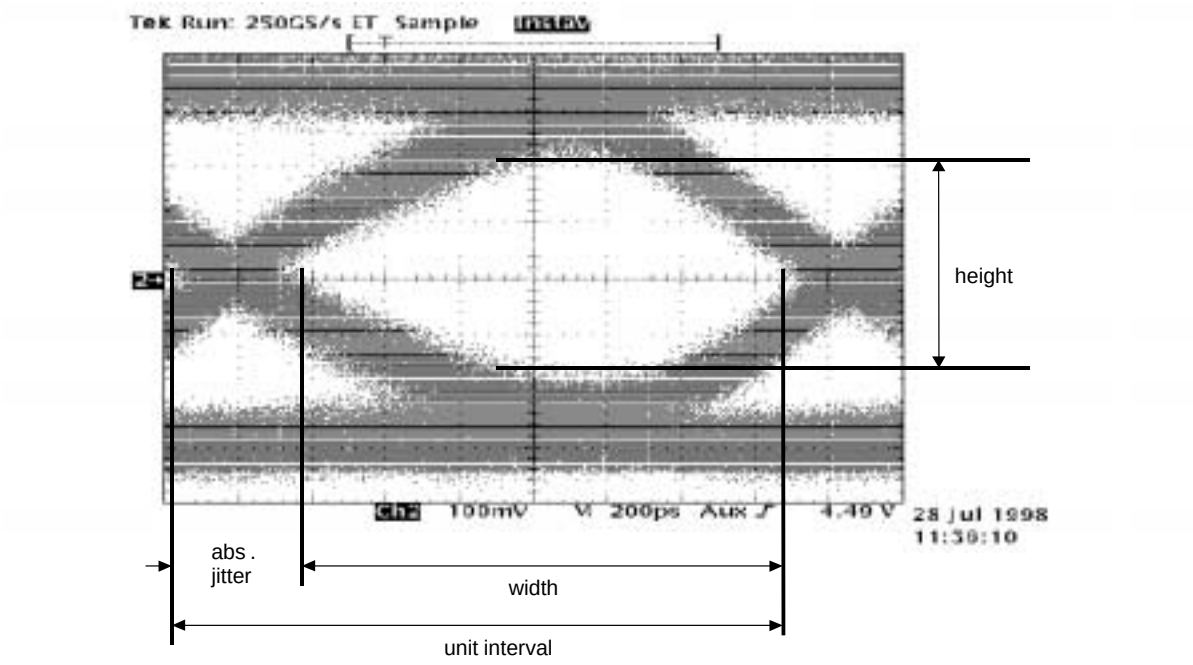


Figure 15. Typical LVDS Eyepattern

A generally accepted range of jitter at the receiver inputs that allows data recovery is 5% to 20% of the unit interval (data pulse width). Table 1 shows the signaling rate achieved on various cables and lengths at a 5% eyepattern jitter with a typical LVDS driver.

Table 1. Signaling Rates for Various Cables for 5% Eyepattern Jitter

LENGTH (m)	CABLE†					
	A (Mbps)	B (Mbps)	C (Mbps)	D (Mbps)	E (Mbps)	F (Mbps)
1	240	200	240	270	180	230
5	205	210	230	250	215	230
10	180	150	195	200	145	180

† Cable A: CAT 3, specified up to 16 MHz, no shield, outside conductor diameter (∅) 0.52 mm
Cable B: CAT 5, specified up to 100 MHz, no shield, ∅ 0.52 mm
Cable C: CAT 5, specified up to 100 MHz, taped over all shield, ∅ 0.52 mm
Cable D: CAT 5 (exceeding CAT 5), specified up to 300 MHz, braided over all shield plus taped individual shield for any pair, ∅ 0.64 mm (AWG22)
Cable E: CAT 5 (exceeding CAT 5), specified up to 350 MHz, ∅ 0.64 mm (AWG22), no shield
Cable F: CAT 5 (exceeding CAT 5), specified up to 350 MHz, “self-shielded”, ∅ 0.64 mm (AWG22)

During synchronous parallel transfers, skew between the data and clock lines will also reduce the timing margin. This must be accounted for in the system timing budget. Fortunately, the low output skew of this LVDS driver will generally be a small portion of this budget.

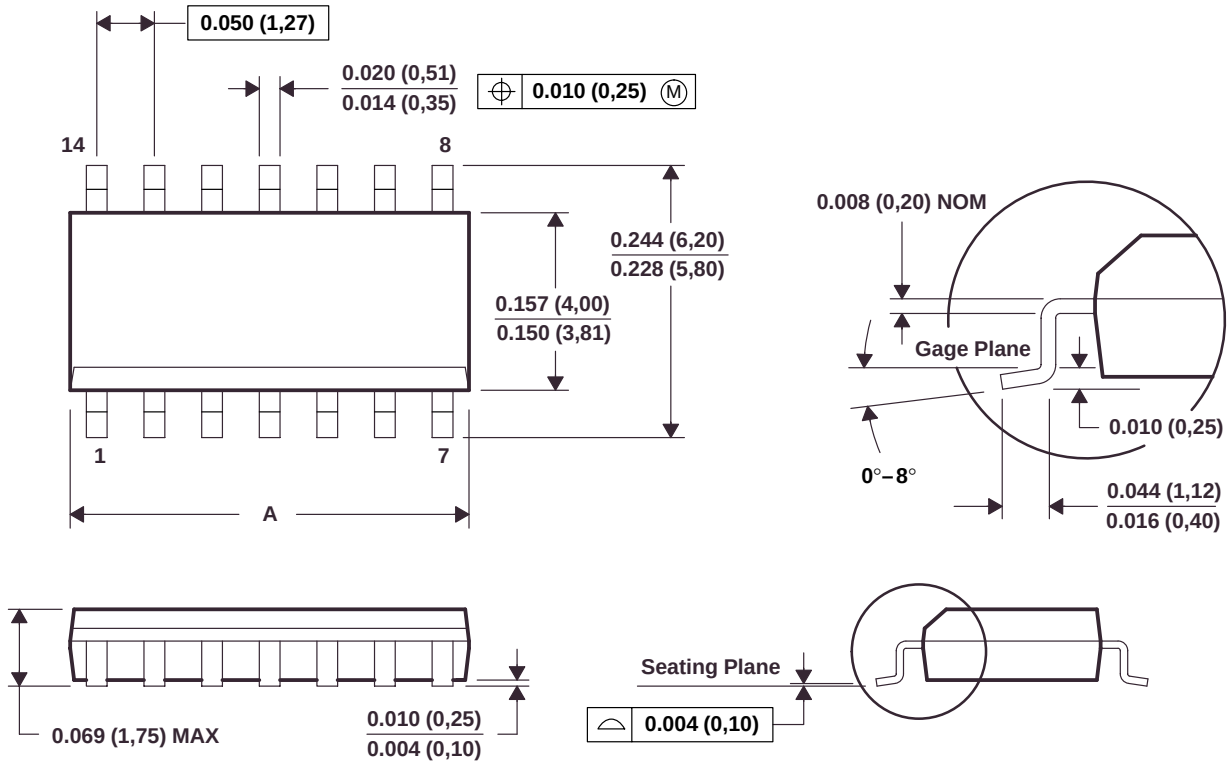
other LVDS products

For other products and applications notes in the LVDS and LVDM product families visit our Web site at **http://www.ti.com/sc/datatran**.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

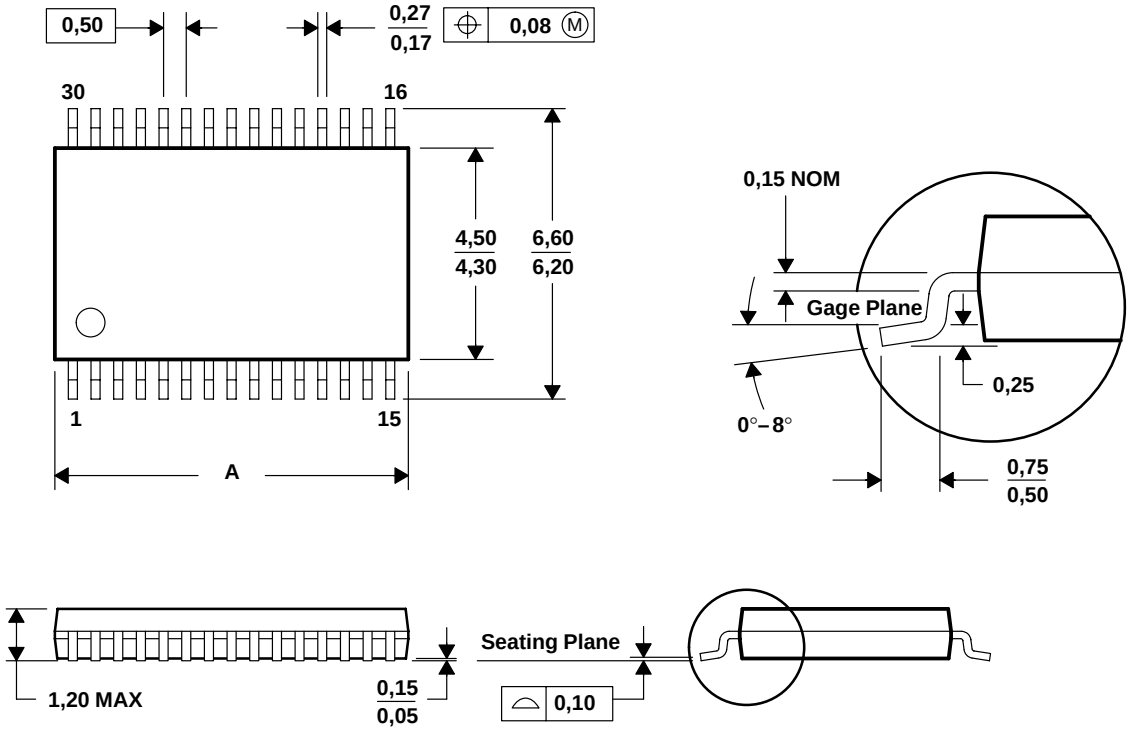
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,10	12,60
A MIN	7,70	7,70	9,60	10,90	12,40

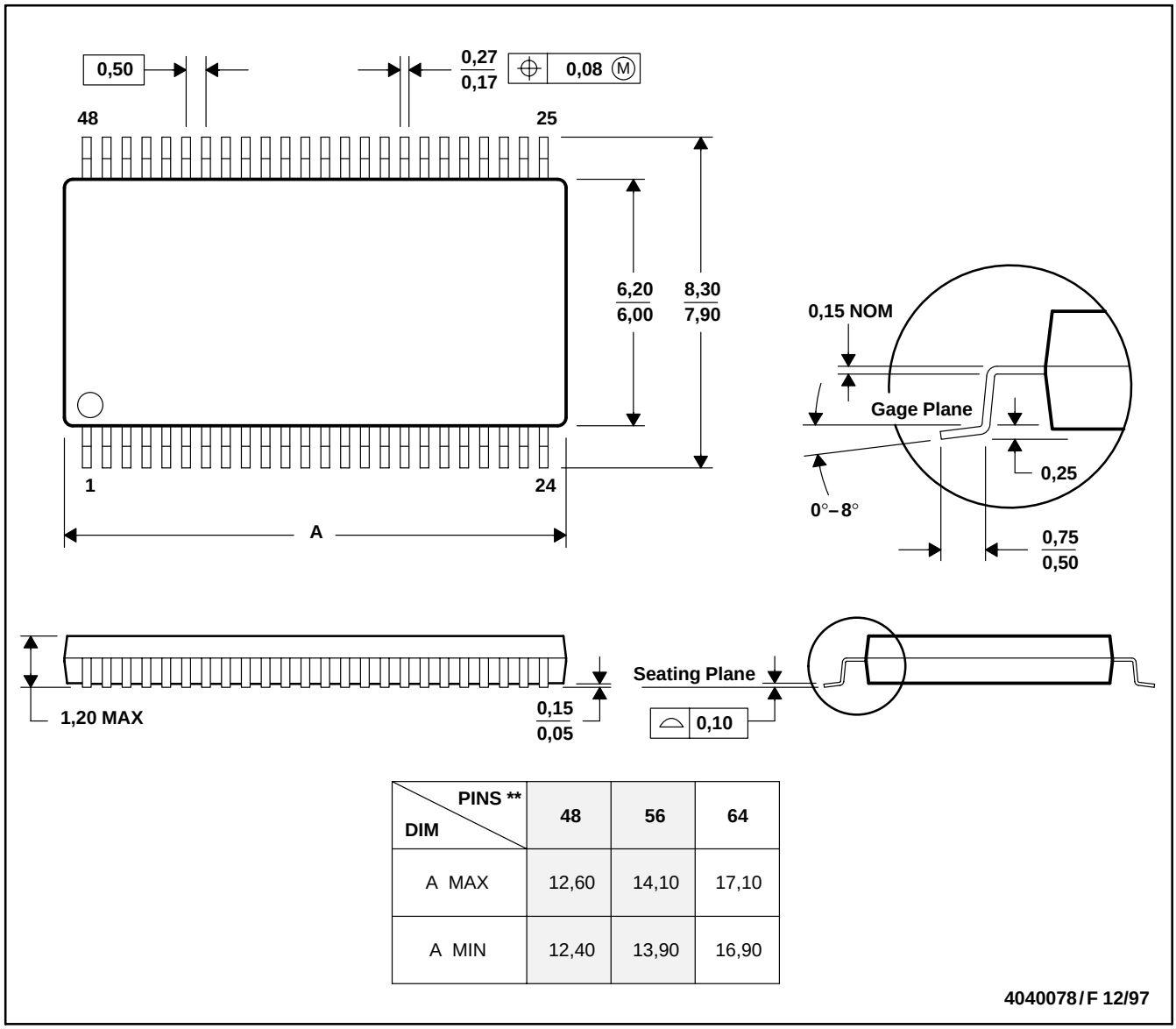
4073252/D 09/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

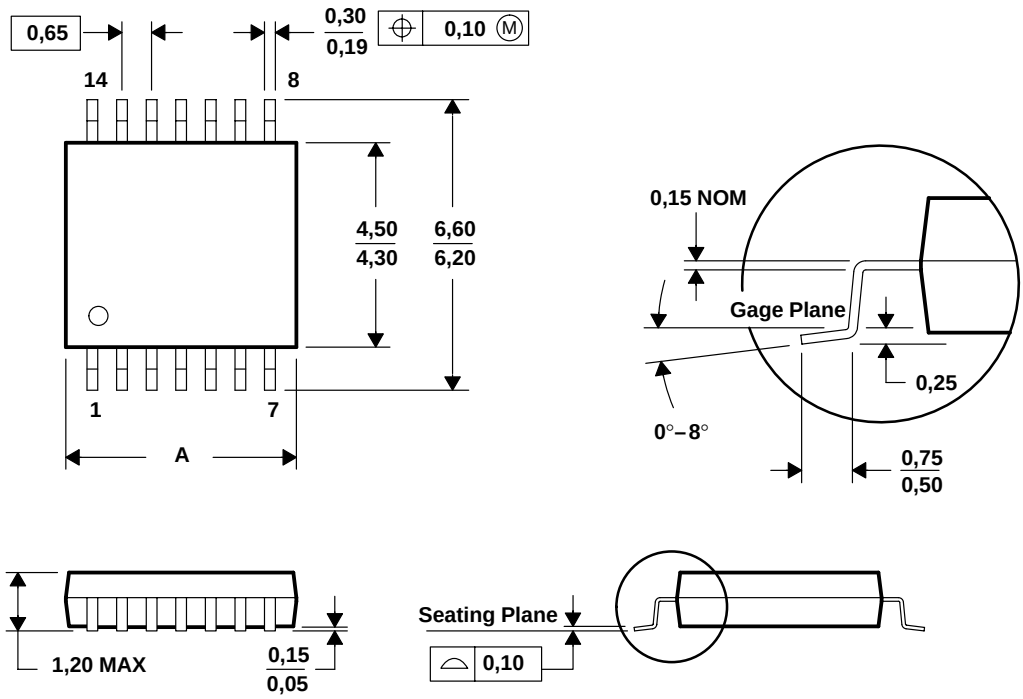
4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265