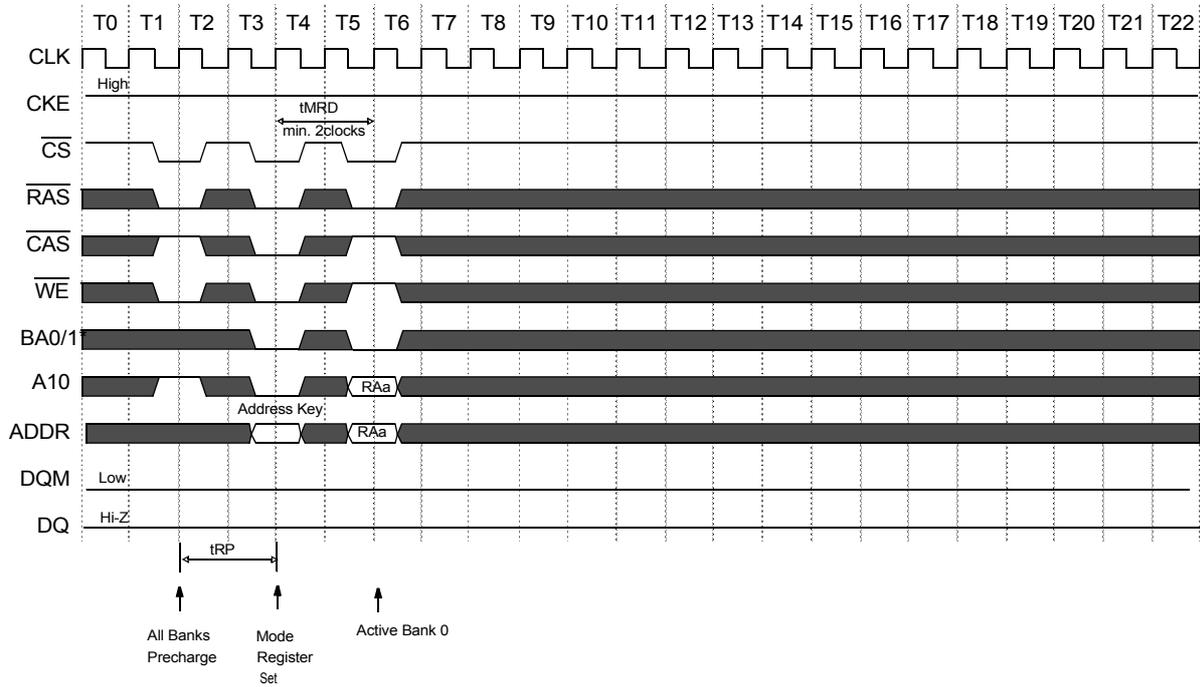


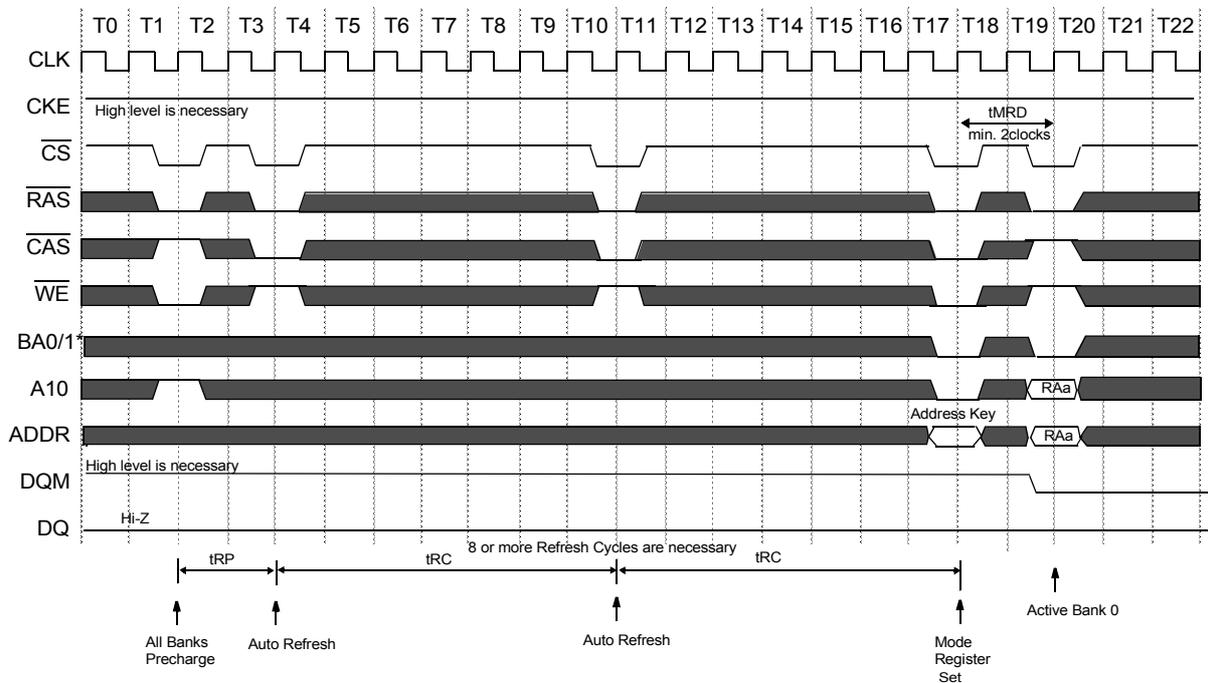
Timing Diagram

- 1 AC Parameters for READ Timing
2. AC Parameters for WRITE Timing
3. Mode Register Set Cycle
4. Power on Sequence and Auto Refresh
5. \overline{CS} Function (Only \overline{CS} Signal needs to be asserted at minimum rate)
6. CKE Timing for Power Down Mode
7. Self-Refresh Entry and Exit
8. CKE Timing for Clock Suspend during Burst READ (BL=4, CL=2)
9. CKE Timing for Clock Suspend during Burst READ (BL=4, CL=3)
10. CKE Timing for Clock Suspend during Burst WRITE (BL=4)
11. Random Column Read (Page with same bank, BL=4, CL=2)
12. Random Column Read (Page with same bank, BL=4, CL=3)
13. Random Column Write (Page with same bank, BL=4, CL=2)
14. Random Column Write (Page with same bank, BL=4, CL=3)
15. Random Row Read (Pingpong banks, BL=8, CL=2)
16. Random Row Read (Pinpong banks, BL=8, CL=3)
17. Random Row Write (Pinpong banks, BL=8, CL=2)
18. Random Row Write (Pinpong banks, BL=8, CL=3)
19. Read and Write DQM Function (BL=4, CL=2)
20. Read and Write DQM Function (BL=4, CL=3)
21. Interleaved Column Read Cycle (BL=4, CL=2)
22. Interleaved Column Read Cycle (BL=4, CL=3)
23. Interleaved Column Write Cycle (BL=4, CL=2)
24. Interleaved Column Write Cycle (BL=4, CL=3)
25. Full Page Read Cycle (CL=2)
26. Full Page Write Cycle (CL=2)
27. Auto Precharge after READ Burst (BL=4, CL=2)
28. Auto Precharge after WRITE Burst (BL=4, CL=2)
29. Test Mode for Read Cycle (BL=4, CL=2)
30. Test Mode for Write Cycle (BL=4, CL=2)

3. Mode Register Set Cycle

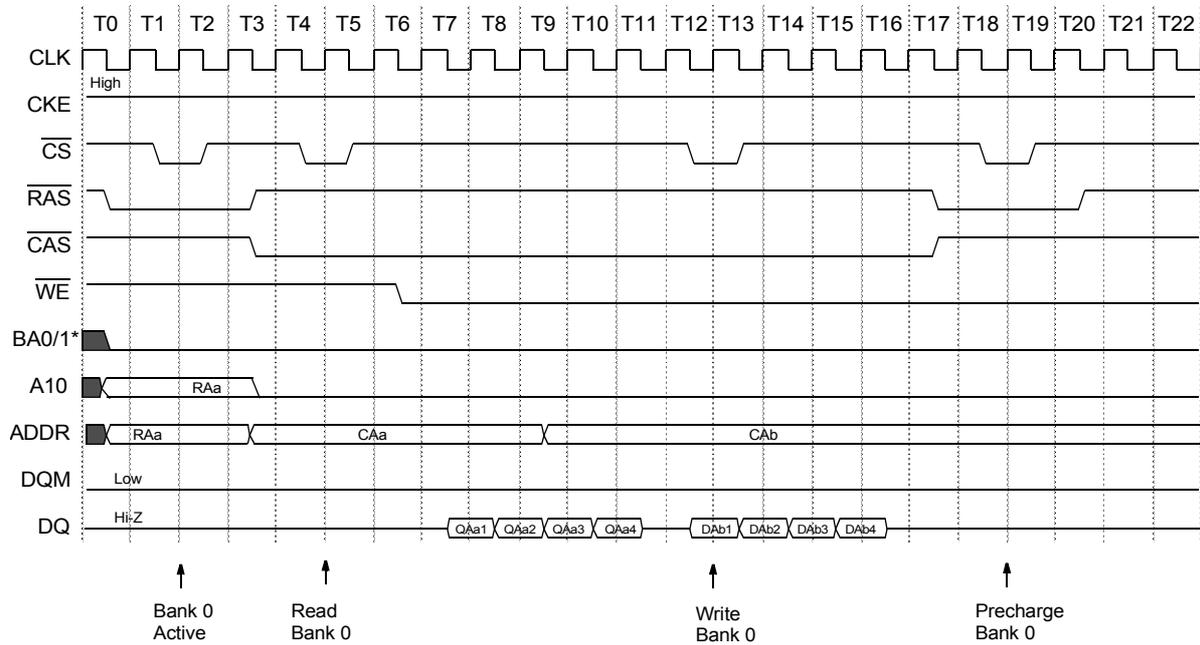


4. Power on Sequence and Auto Refresh

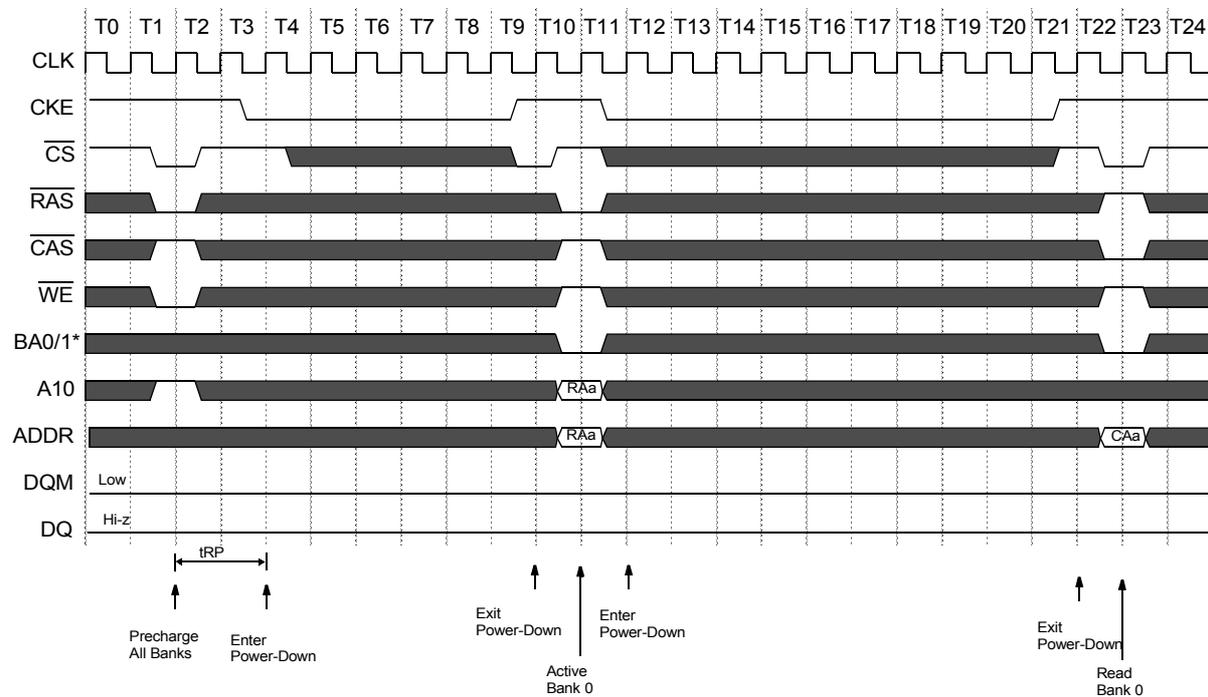


Note* : The 16M Synchronous DRAM Series have one BA.

5. \overline{CS} Function (Only \overline{CS} signal needs to be asserted at min. rate) : BL=4, CL=3

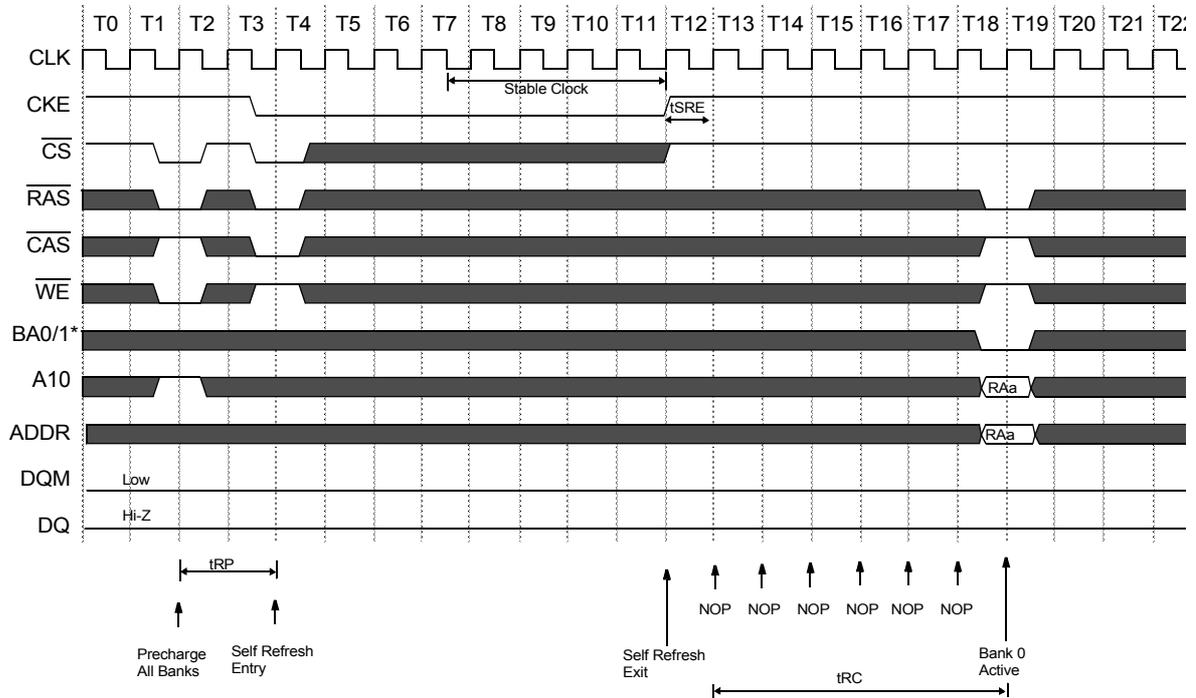


6. CKE Timing for Power Down Mode

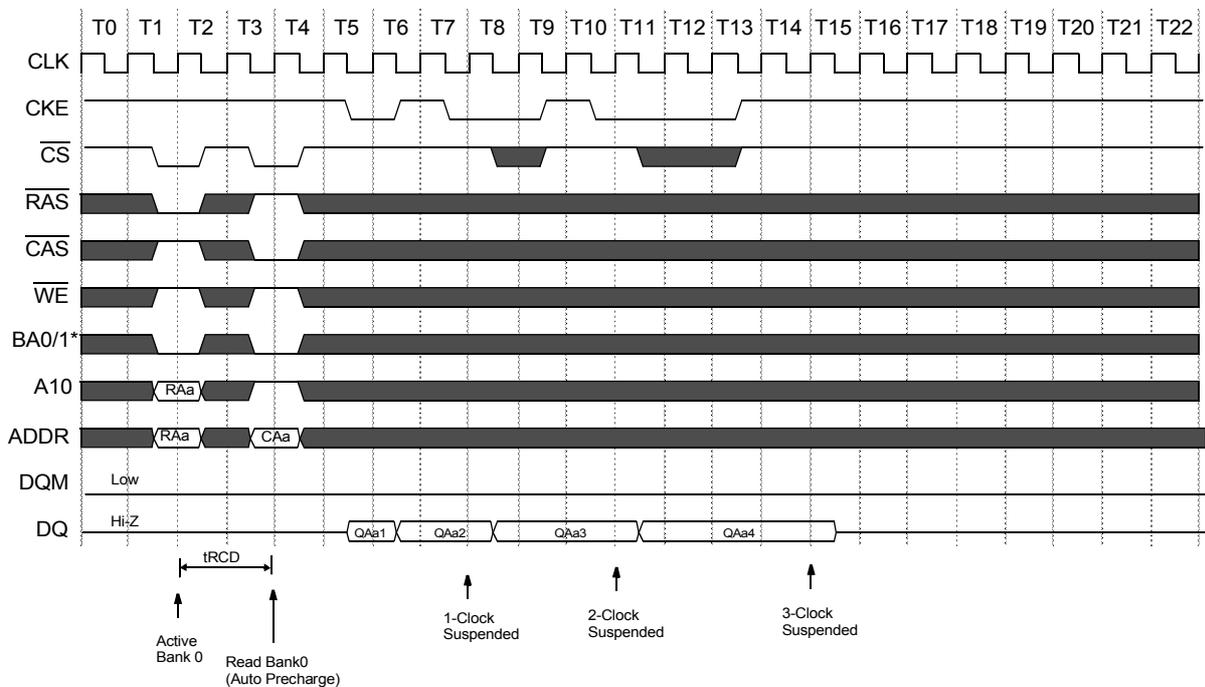


Note* : The 16M Synchronous DRAM Series have one BA.

7. Self Refresh Entry and Exit

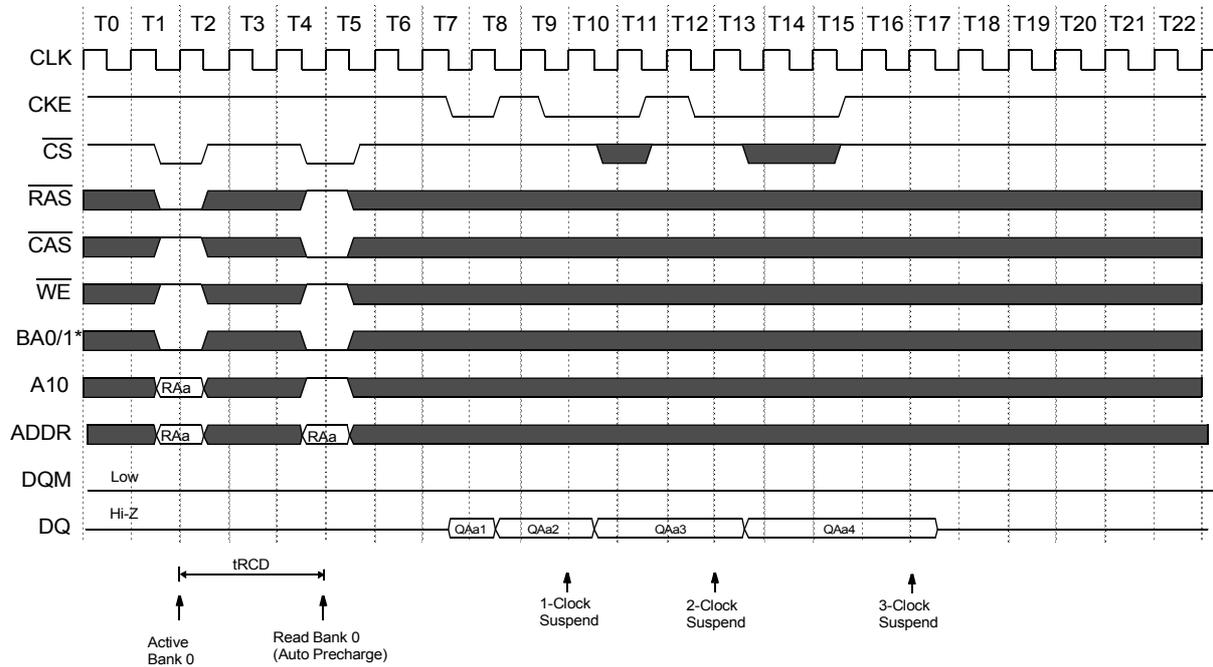


8. CKE Timing for Clock Suspend during Burst READ : BL=4, CL=2

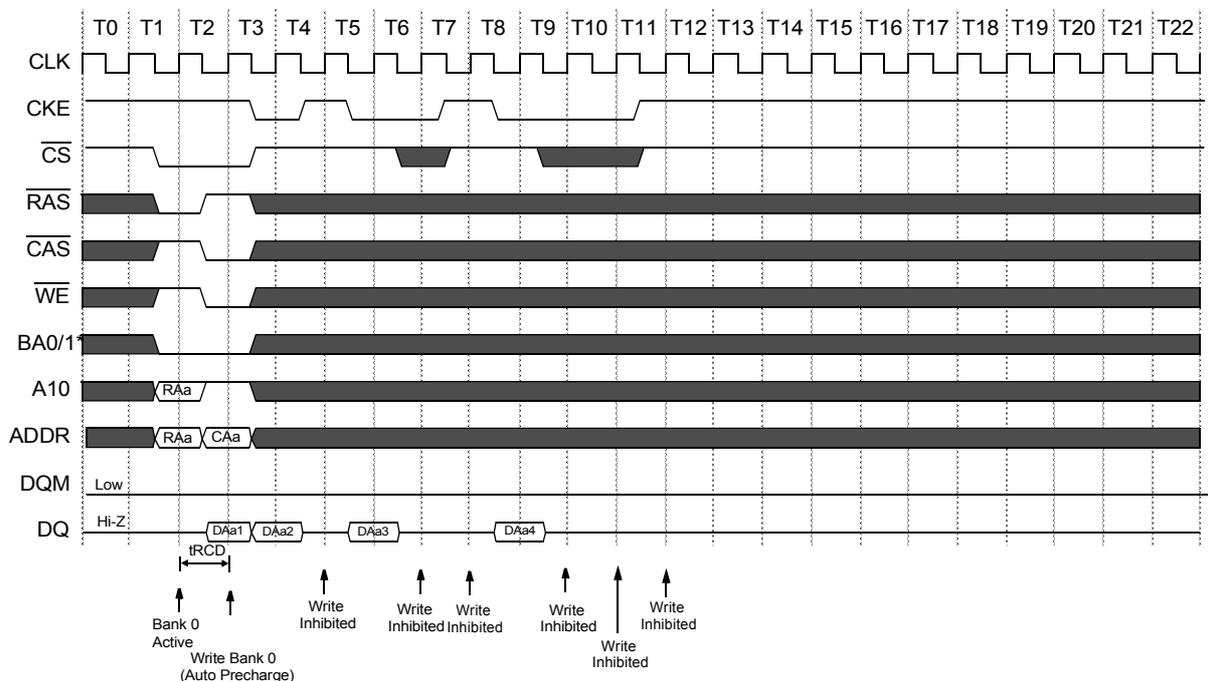


Note* : The 16M Synchronous DRAM Series have one BA.

9. CKE Timing for Clock Suspend during Burst READ : BL=4, CL=3

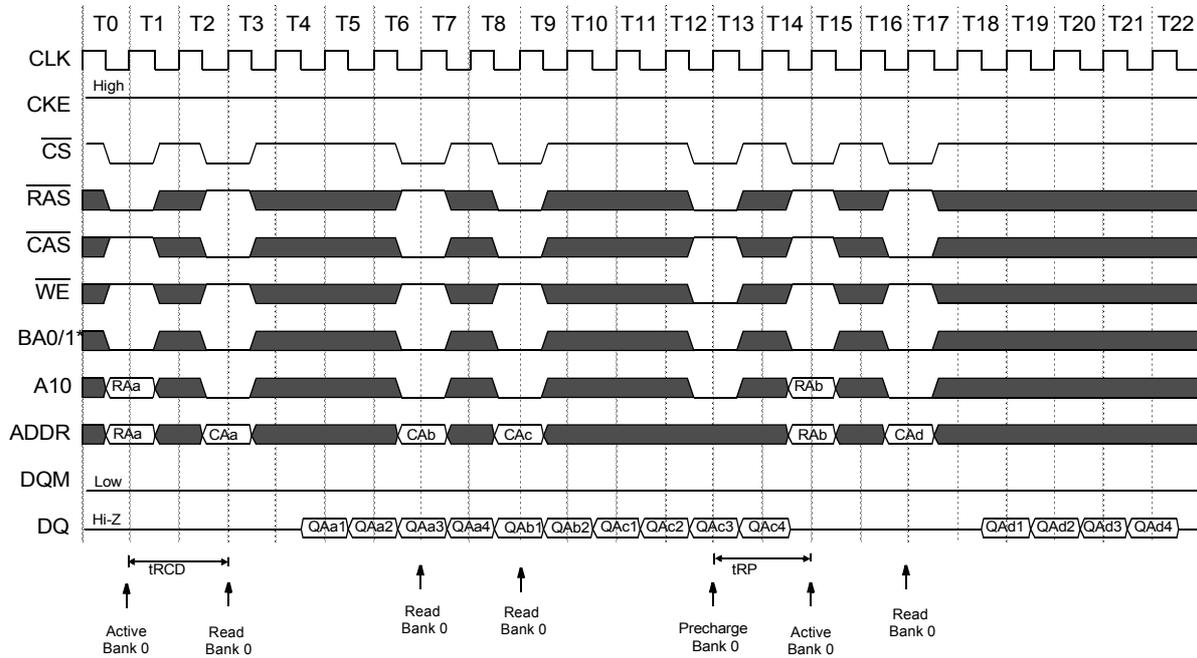


10. CKE Timing for Clock Suspend during Burst WRITE : BL=4

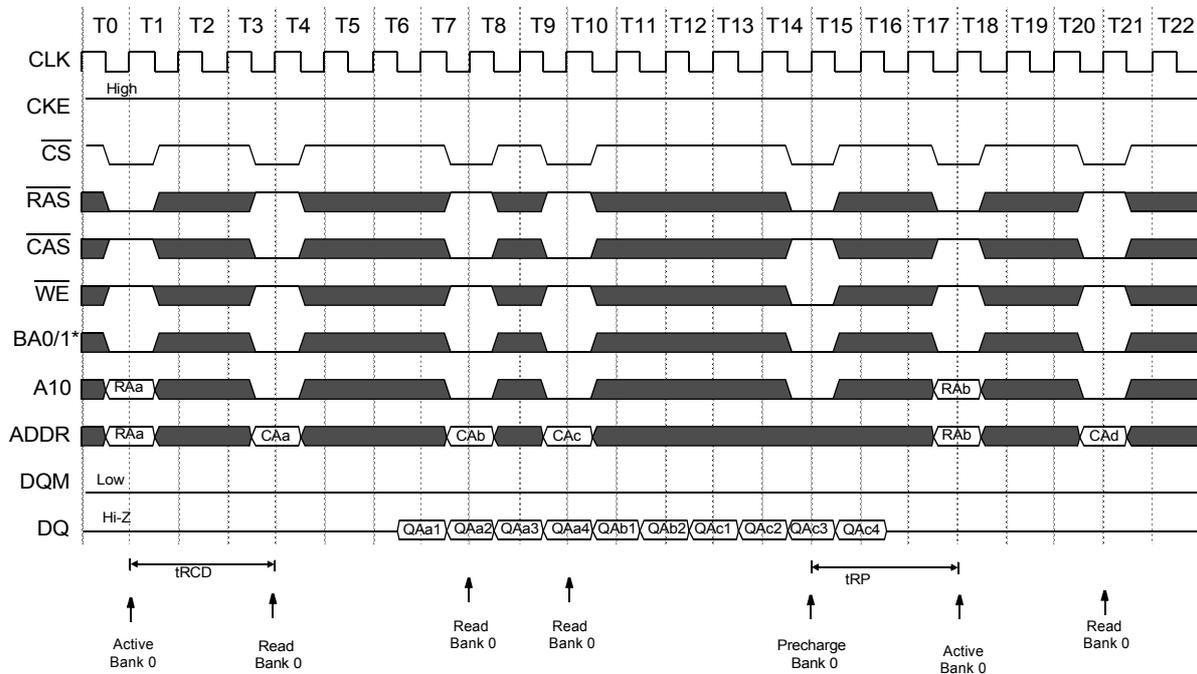


Note* : The 16M Synchronous DRAM Series have one BA.

11. Random Column Read (Page with same bank) : BL=4, CL=2

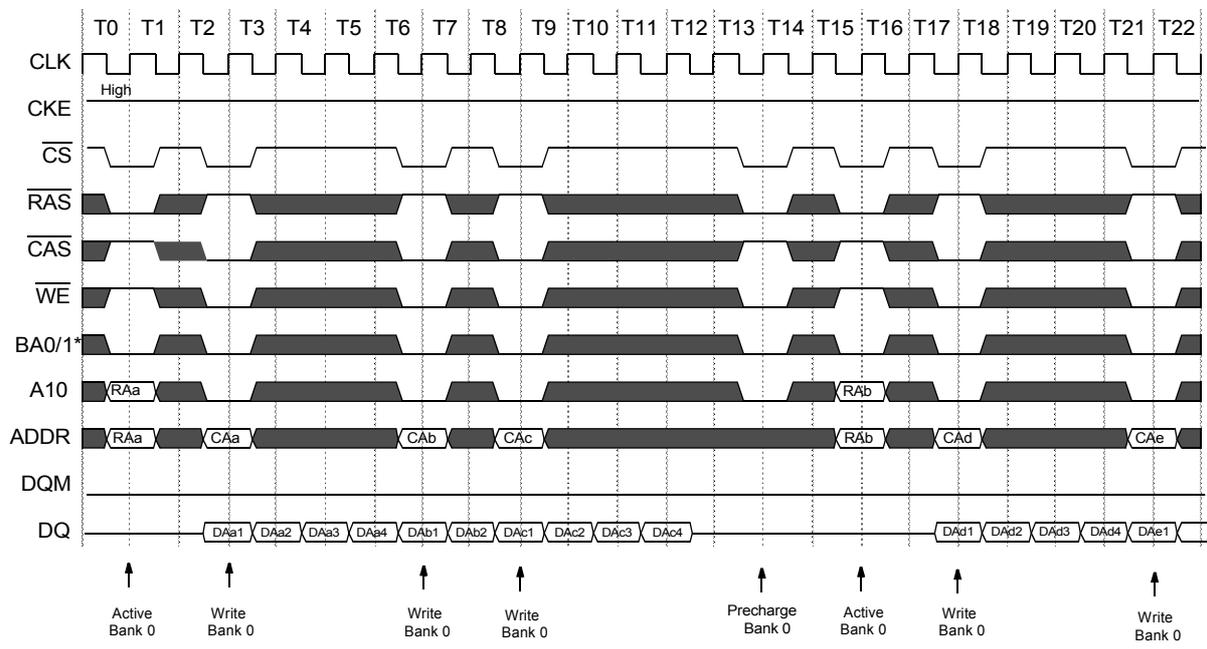


12. Random Column Read (Page with same bank) : BL=4, CL=3

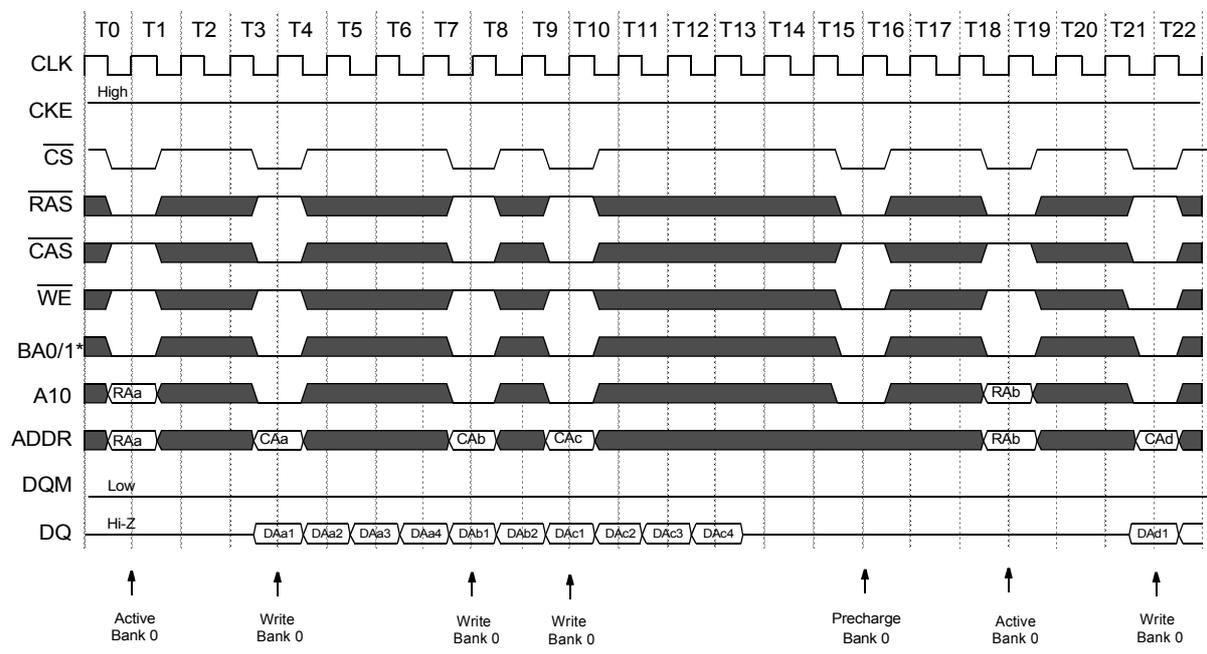


Note* : The 16M Synchronous DRAM Series have one BA.

13. Random Column Write (Page with same bank) : BL=4, CL=2

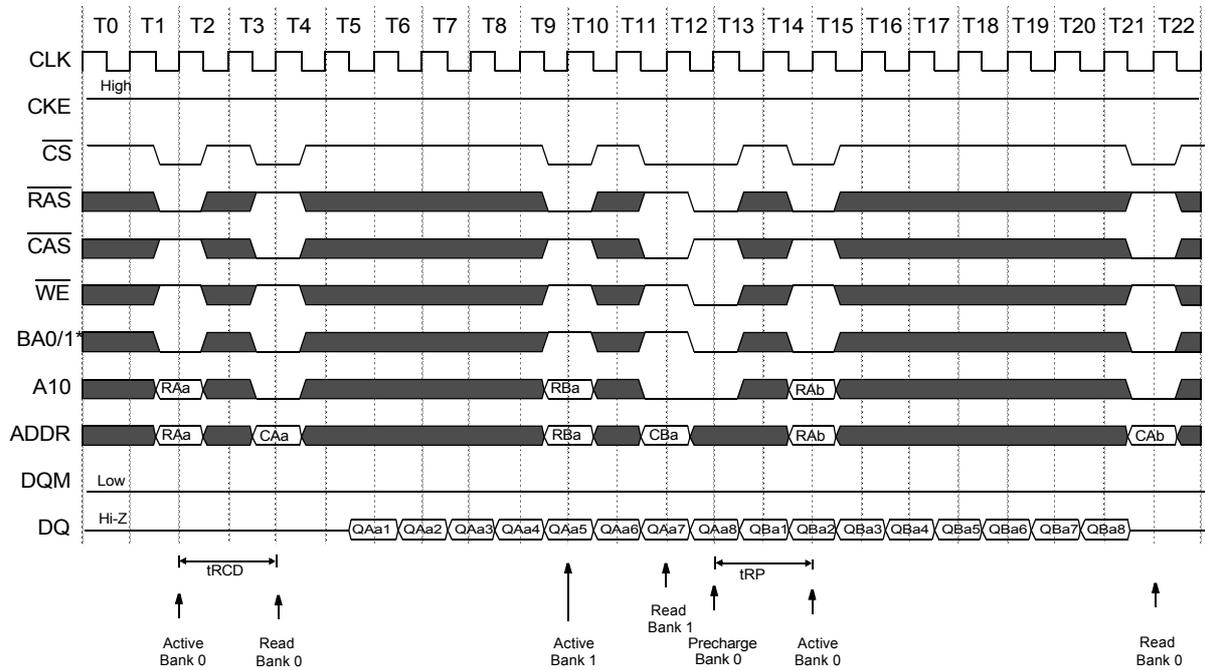


14. Random Column Write (Page with same bank) : BL=4, CL=3

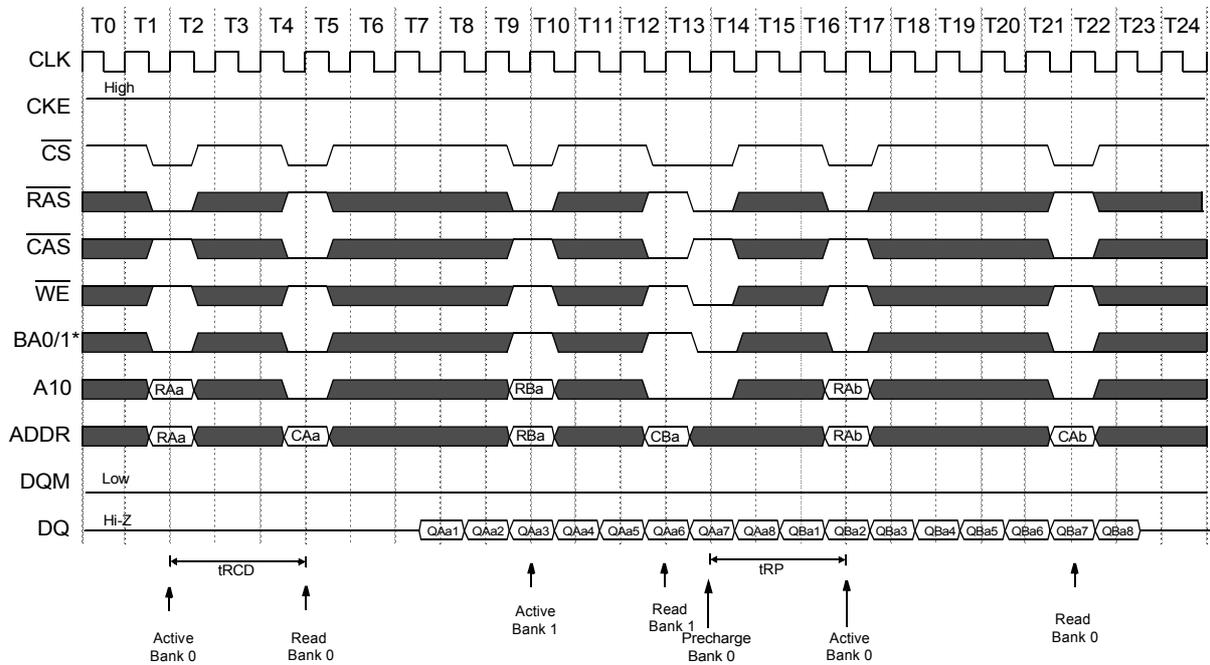


Note* : The 16M Synchronous DRAM Series have one BA.

15. Random Row Read (Pingpong banks) : BL=8, CL=2

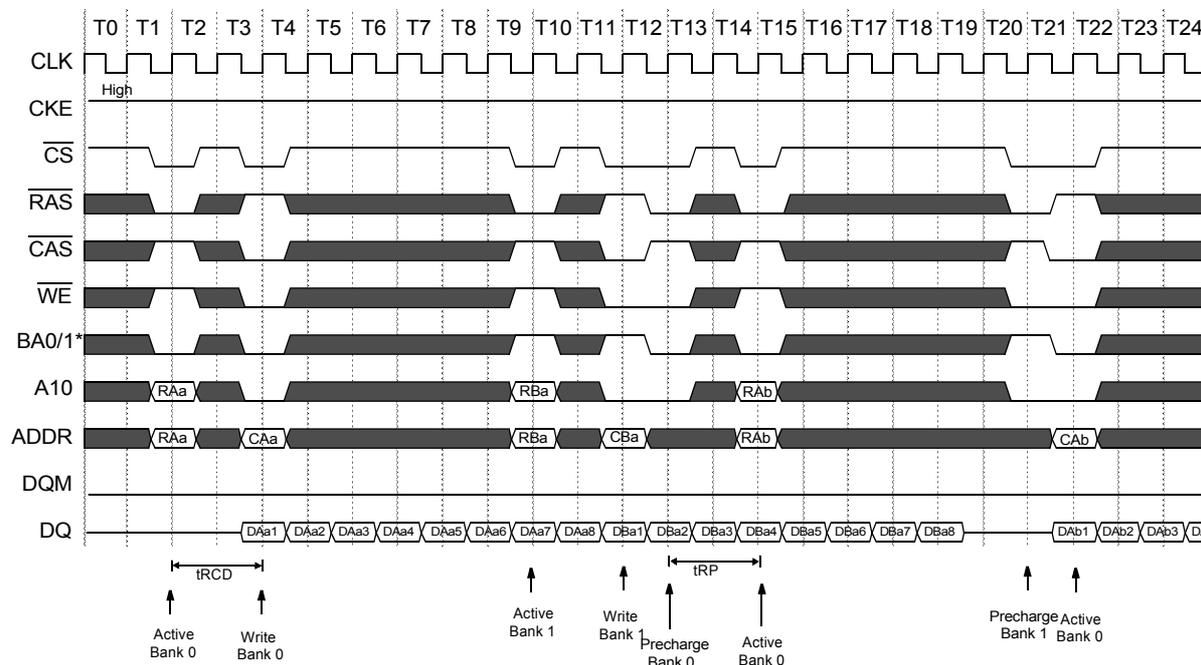


16. Random Row Read (Pinpong banks) : BL=8, CL=3

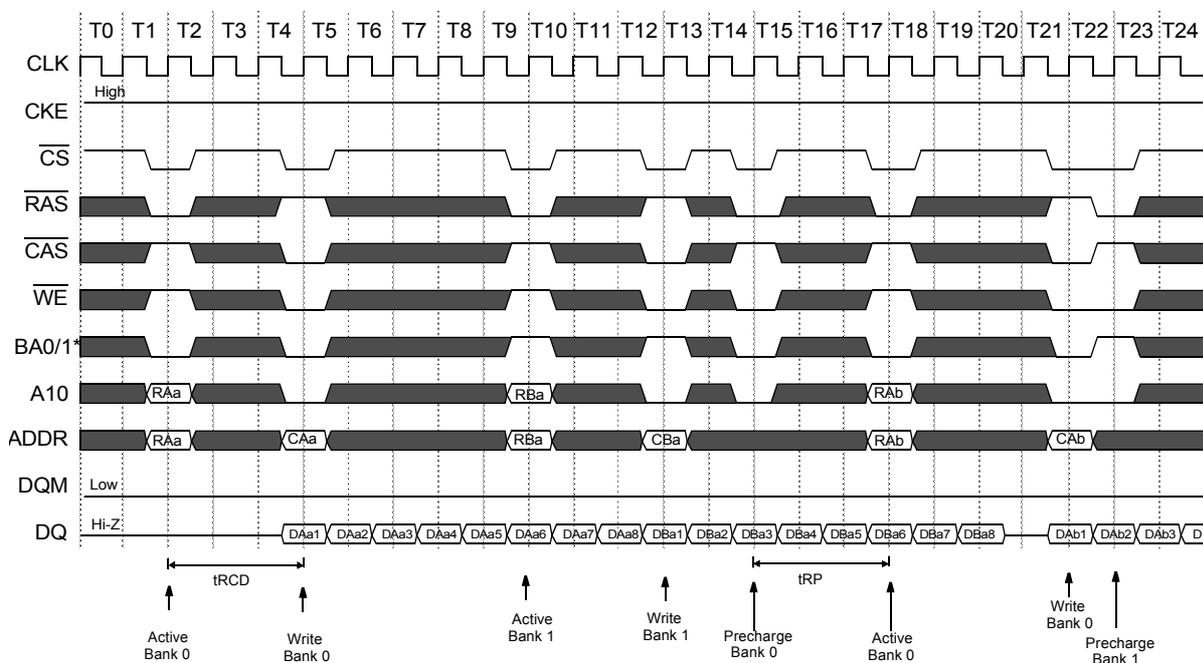


Note* : The 16M Synchronous DRAM Series have one BA.

17. Random Row Write (Pingpong banks) : BL=8, CL=2

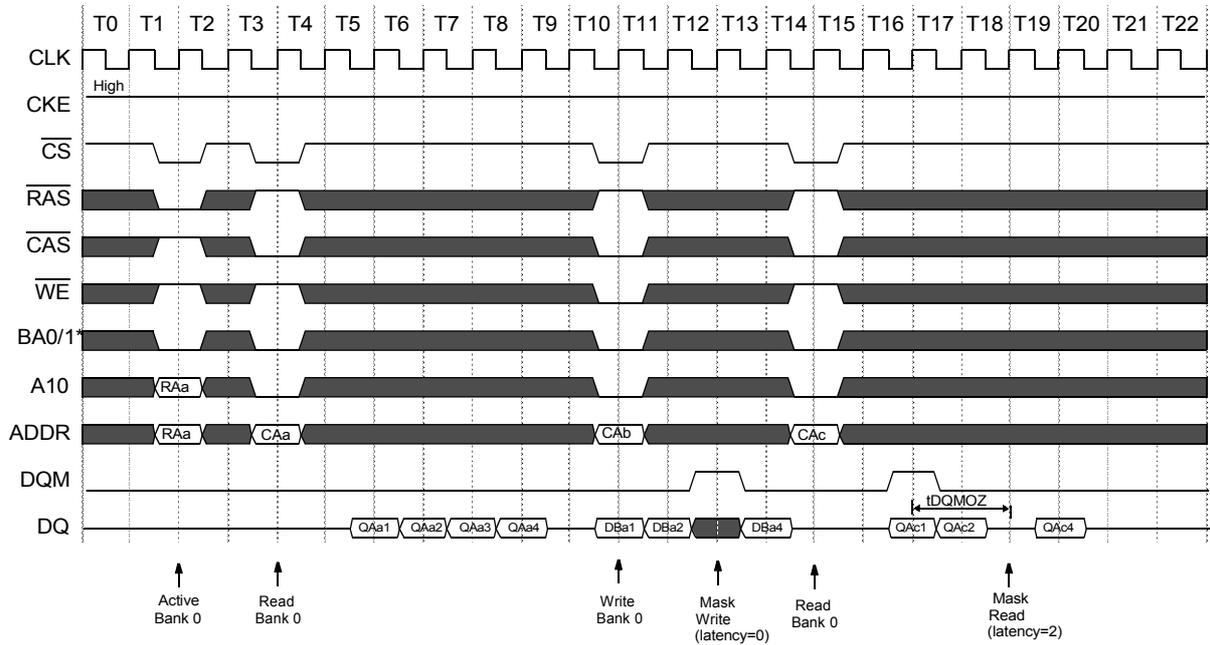


18. Random Row Write (Pingpong banks) : BL=8, CL=3

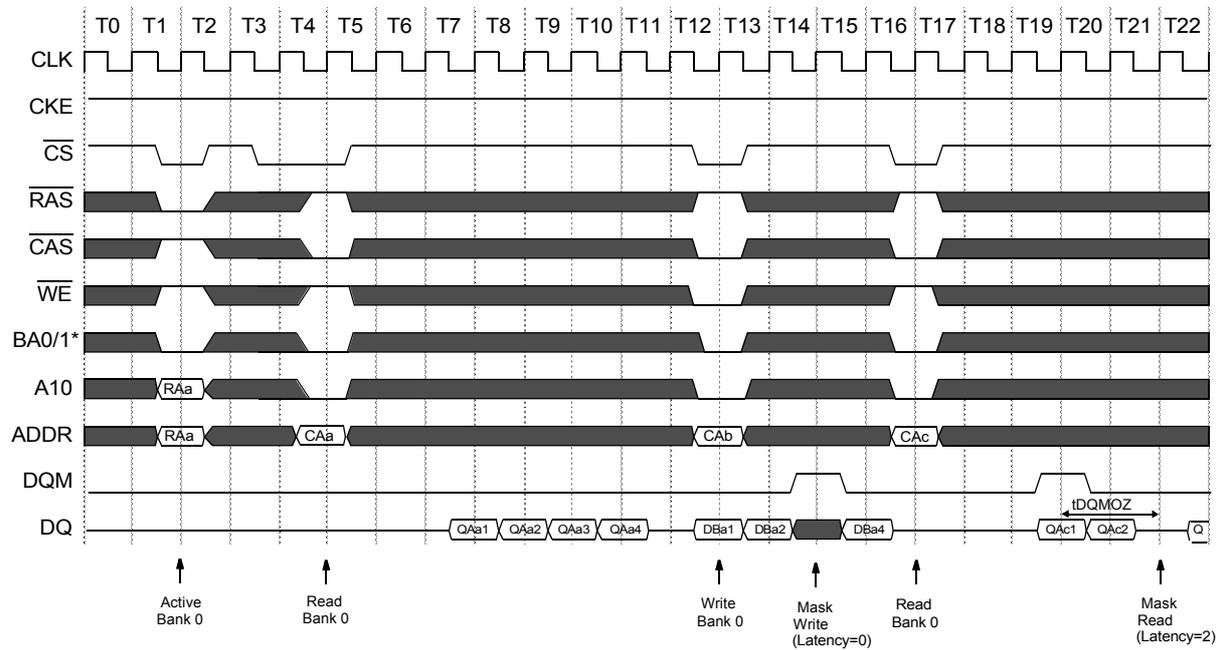


Note* : The 16M Synchronous DRAM Series have one BA.

19. Read and Write with DQM Function : BL=4, CL=2

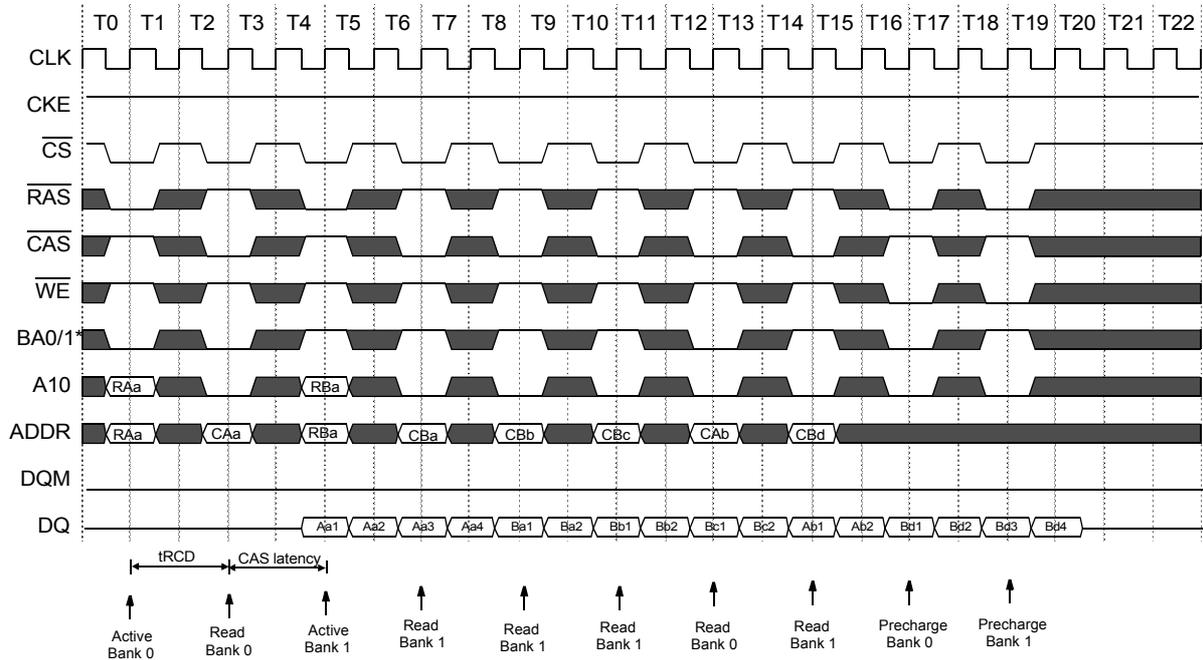


20. Read and Write with DQM Function : BL=4, CL=3

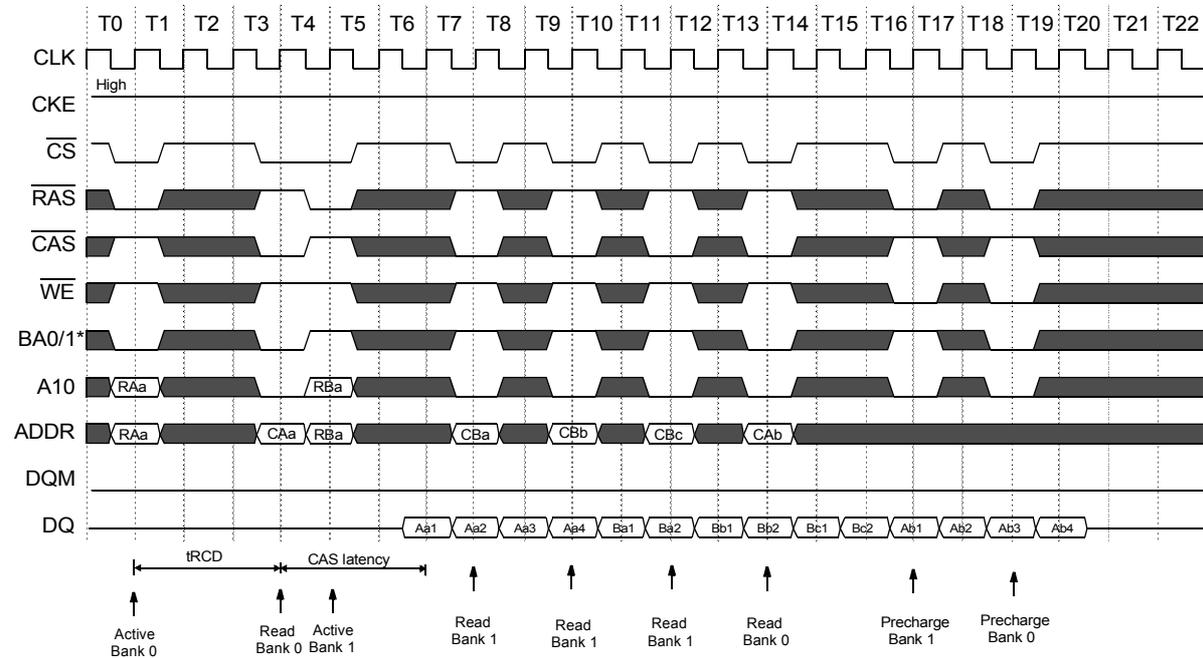


Note* : The 16M Synchronous DRAM Series have one BA.

21. Interleaved Column Read Cycle : BL=4, CL=2

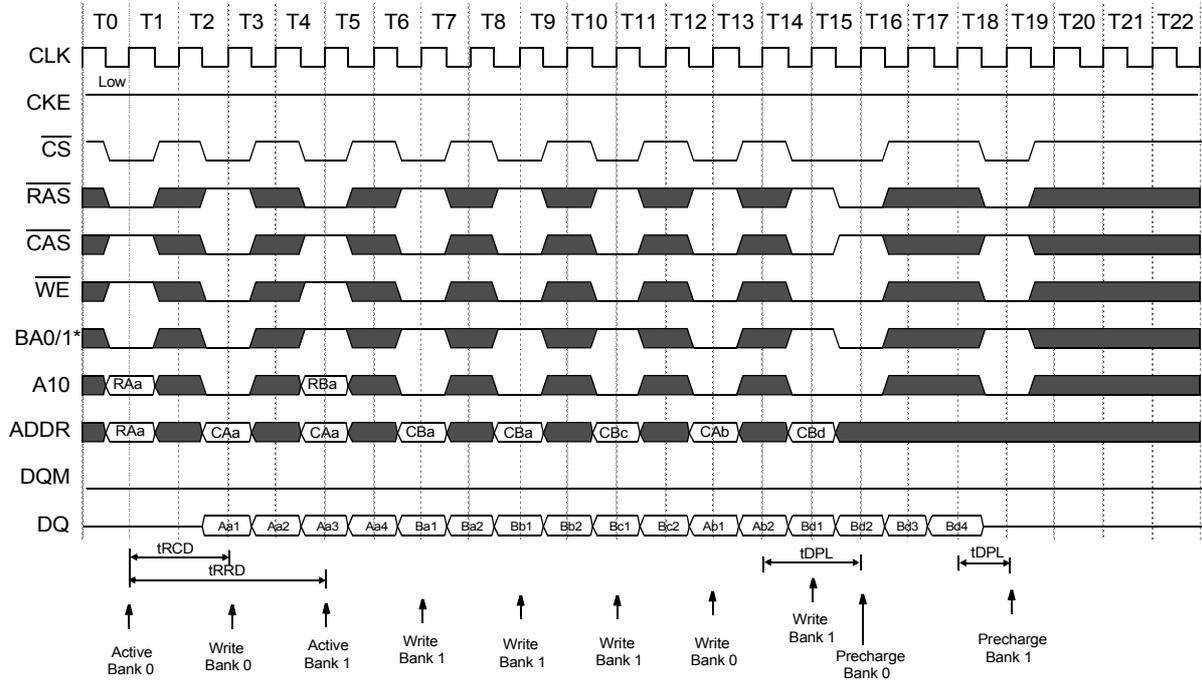


22. Interleaved Column Read Cycle : BL=4, CL=3

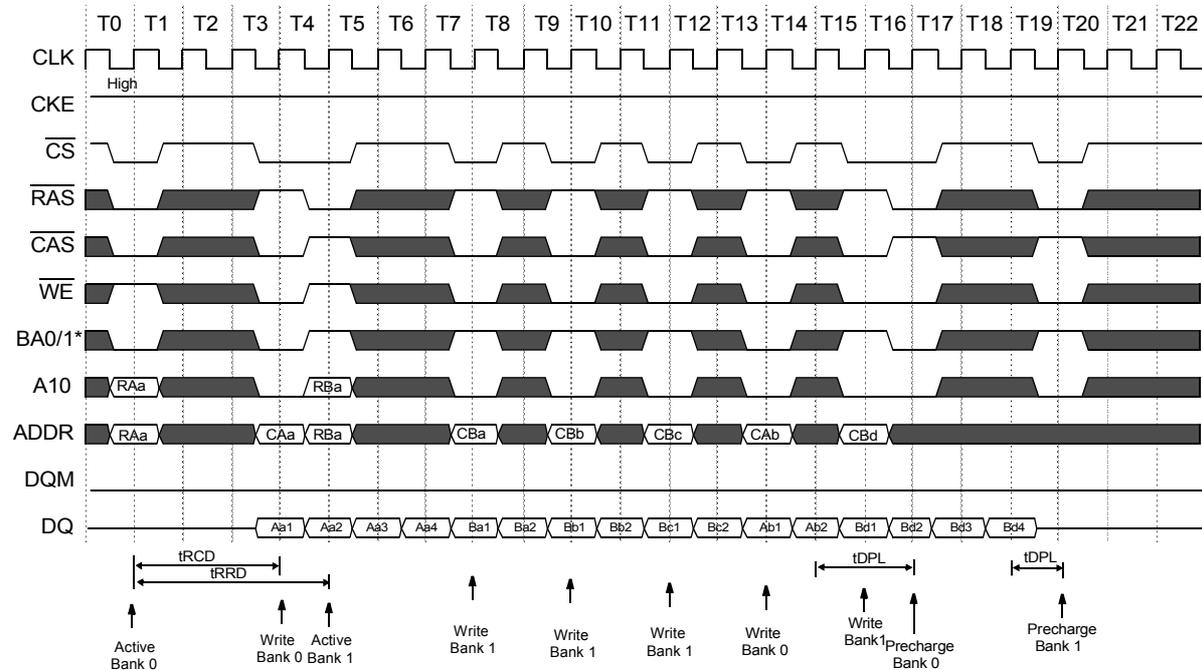


Note* : The 16M Synchronous DRAM Series have one BA.

23. Interleaved Column Write Cycle : BL=4, CL=2

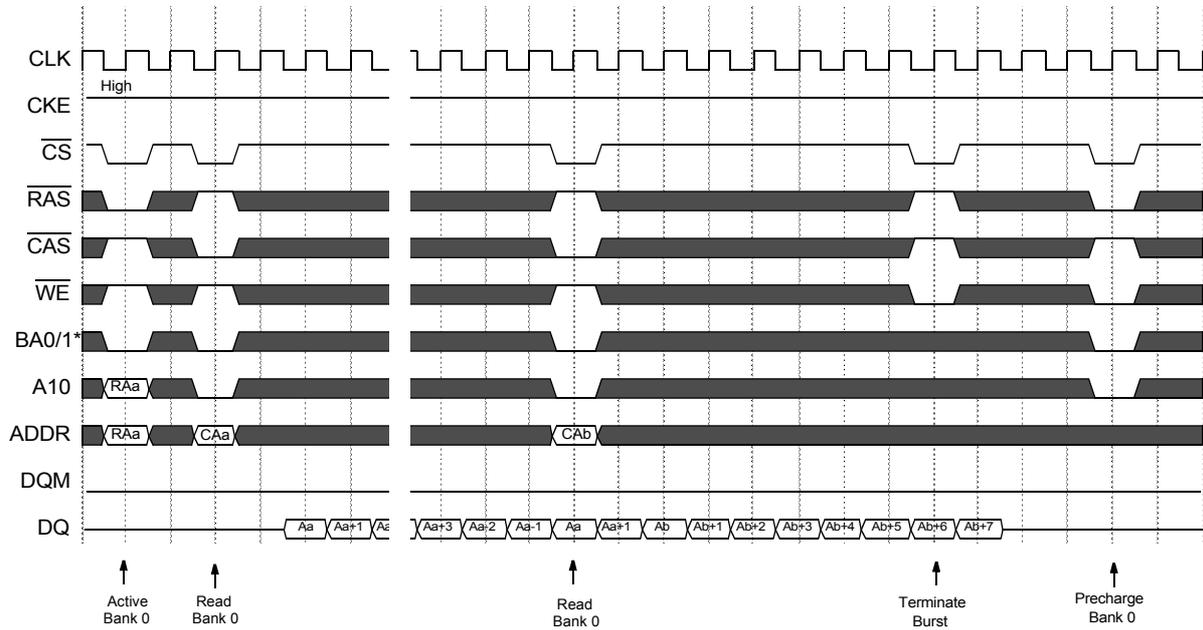


24. Interleaved Column Write Cycle : BL=4, CL=3

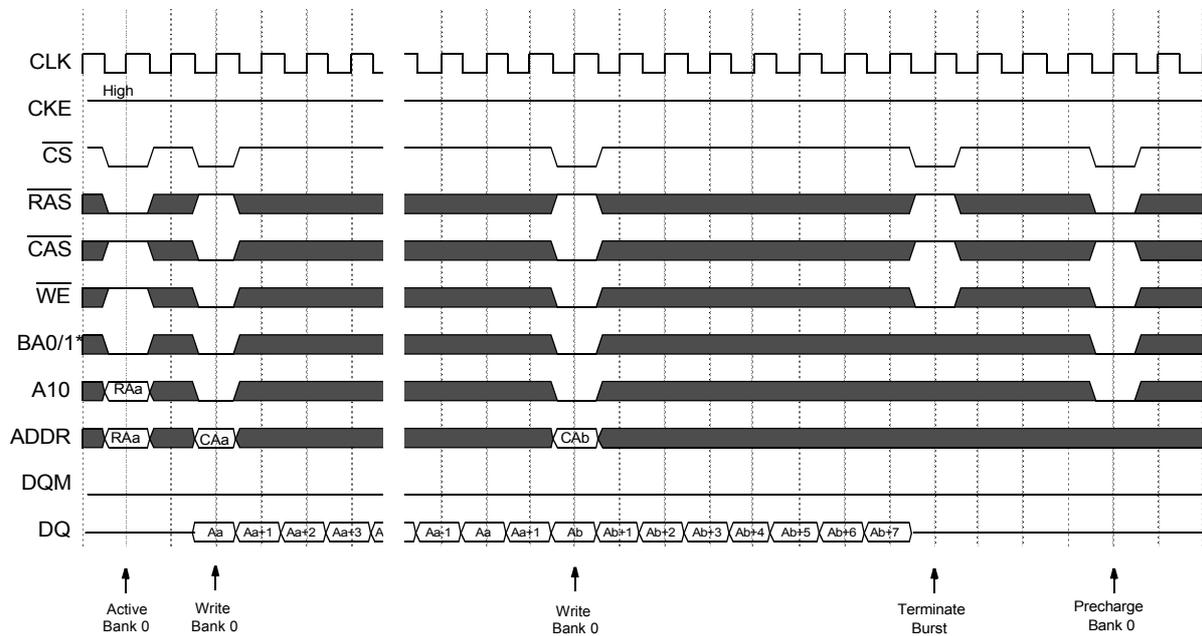


Note* : The 16M Synchronous DRAM Series have one BA.

25. Full Page Read Cycle : CL=2

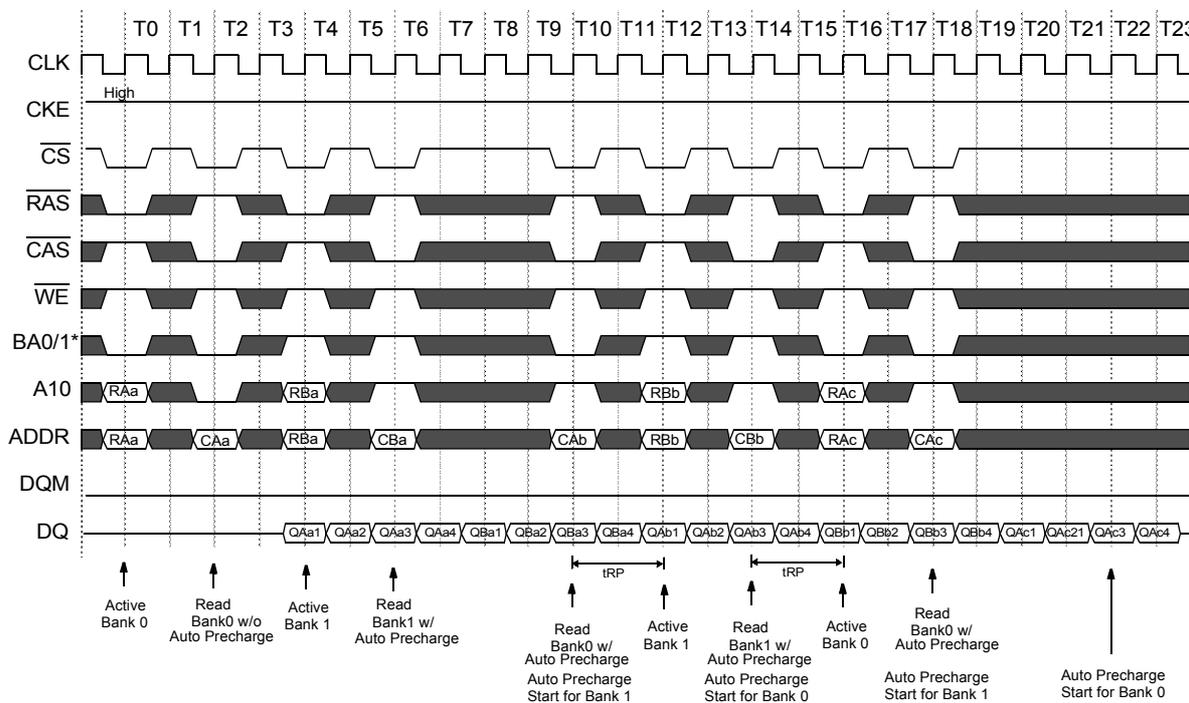


26. Full Page Write Cycle : CL=2

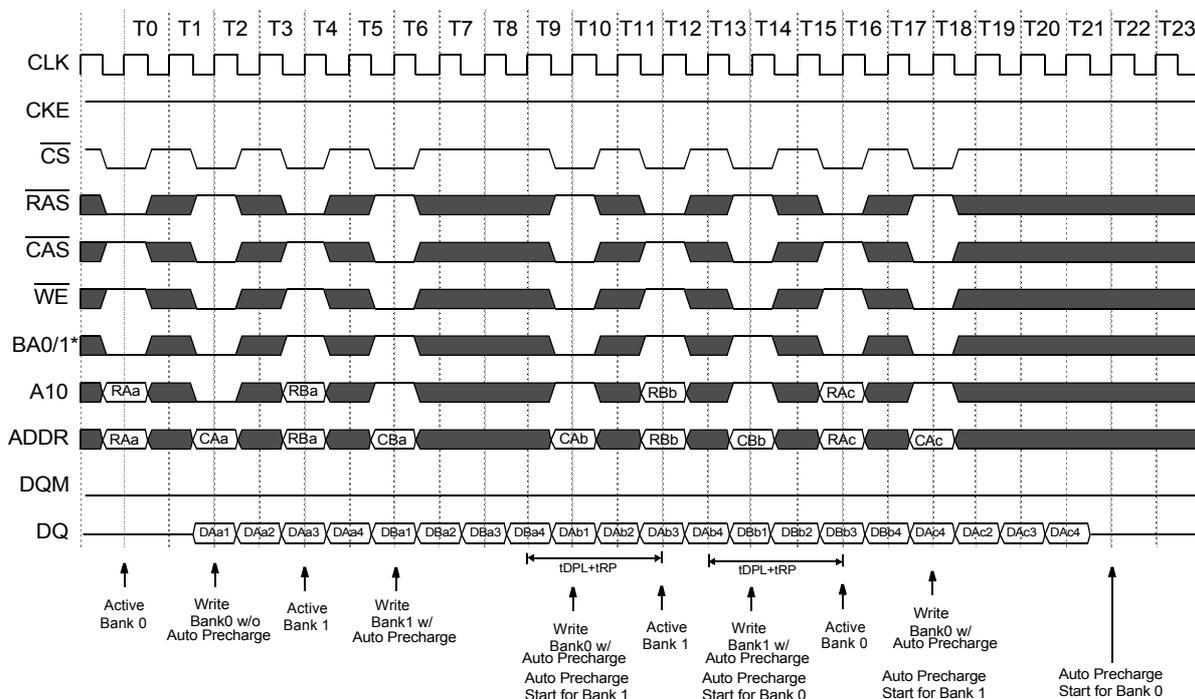


Note* : The 16M Synchronous DRAM Series have one BA.

27. Auto Precharge after Read Burst : BL=4, CL=2

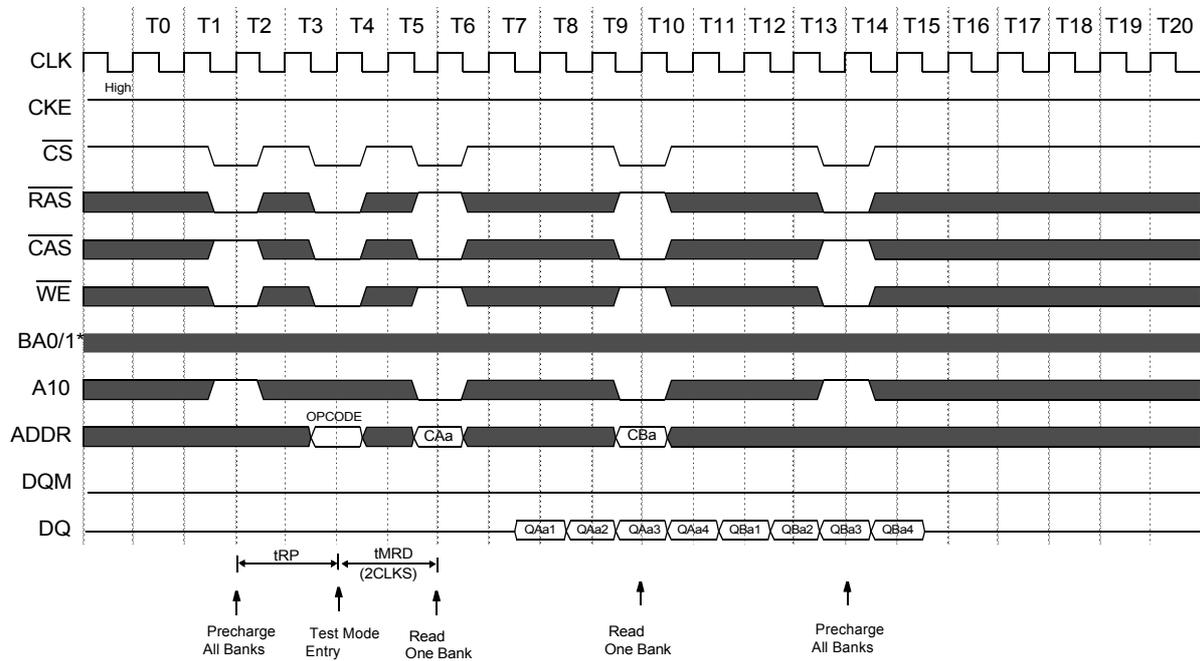


28. Auto Precharge after Write Burst : BL=4, CL=2

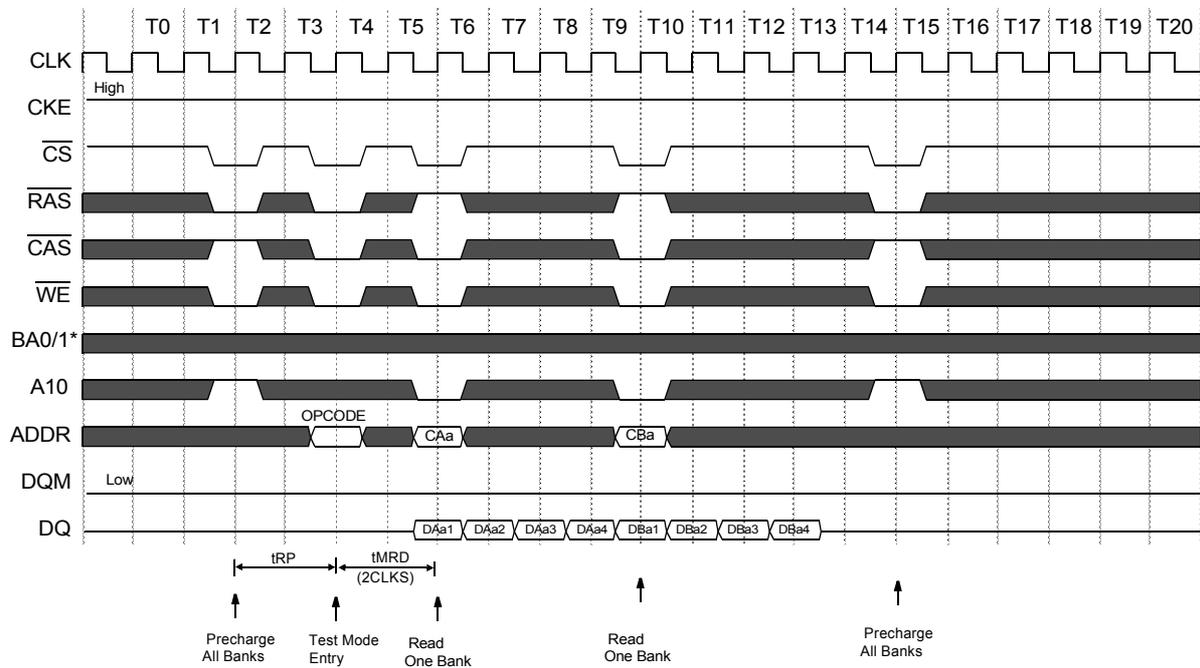


Note* : The 16M Synchronous DRAM Series have one BA.

29. Test Mode for Read Cycle : BL=4, CL=2



30. Test Mode for Write Cycle : BL=4, CL=2



Note* : The 16M Synchronous DRAM Series have one BA.