TECHNICAL NOTE

INITIALIZATION SEQUENCE FOR DDR SDRAM

Introduction

SDRAM is a volatile and complex memory device. That is, when the power is removed, all contents and operating configurations are lost. Each time the memory is powered up, the device requires a defined procedure to initialize the internal state machines and to configure the various user defined operating parameters.

This technical note concentrates on the flow for the initialization sequence and the configurable device parameters.

Initializing DDR SDRAM

To ensure device functionality a predefined sequence must occur at device power-up or in conjunction with a power-on reset.

Step 1

Provide power. The device core power (V_{DD}) and device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. At all times, V_{DDQ} must be greater than or equal to V_{IN} (DC) MAX. Although not required, both V_{DD} and V_{DDQ} are typically from the same power source.

Step 2

Apply the reference voltage (V_{REF}), then the termination voltage (V_{TT}). The reference voltage may ramp anytime after V_{DDQ} and should always be equal to $V_{DDQ}/2$. During ramp, it is extremely important that the voltage at the device I/O pin does not exceed that of V_{DDQ}. Typically, the termination resistors will provide an IR drop between the actual V_{TT} levels and input voltage at the DRAM input.

Step 3

Assert and hold clock enable (CKE) to a LVCMOS logic LOW level. During the initial power ramp, the CKE input will not recognize SSTL_2 logic levels. A LOW level on CKE will prevent unwanted commands to be received by the DRAM and will keep the DRAM from driving the I/O pins.

Step 4

Once the system has established reliable device power and CKE has been driven LOW, it is safe to apply a stable clock.

Step 5

There must be at least 200µs of valid clocks before any command may be given to the DRAM.

Step 6

To initialize the internal logic of the DRAM, bring CKE to a SSTL_2 logic HIGH and assert either a NOP or DESELECT on the command bus. Note, at this point, the CKE input transitions from a LVCMOS input to a SSTL_2 input only and will remain an SSTL_2 input.

Step 7

Assert a PRECHARGE ALL command.

Step 8

Provide NOPs or DESELECT commands for at least ^{t}RP.

Step 9

Using the LMR command, program the extended mode register. At this point, the DLL must be configured (set E0 = 0 to enable the DLL) and the I/O drive strength (set E1 = 1 for standard drive or E1 = 0 for reduced drive levels). All other bits must be set to zero.

Step 10

Provide NOPs or DESELECT commands for at least ^{t}MRD.

Step 11

Using the LMR command, program the mode register for the desired operating modes. Note, all MR bits other than M0 through M7 must be set to zero. This step also performs a DLL reset. Anytime a DLL reset occurs, 200 clock cycles must be provided before any READ command may be issued.

Step 12

Provide NOPs or DESELECT commands for at least ^{t}MRD.

Step 13

Issue a PRECHARGE ALL command with A10 set to a logic HIGH level.

Step 14

Provide NOPs or DESELECT commands for at least ^{t}RP.

Step 15

Issue an AUTO REFRESH command. Note, as part of the initialization sequence, there must be two AUTO REFRESH commands issued. The standard flow is to issue one at Step 15 and one at Step 17. Alternately, these may occur anytime after Step 10.

Step 16

Provide NOPs or DESELECT commands for at least ^{t}RFC.

Step 17

Issue the second AUTO REFRESH command.

Step 18

Provide NOPs or DESELECT commands for at least ^{t}RFC.

Step 19

Although not required for Micron® devices, JEDEC requires an LMR command to clear the DLL bit (set M8 = 0). If a LMR command is issued, the same operating parameters should be set as configured in Step 11.

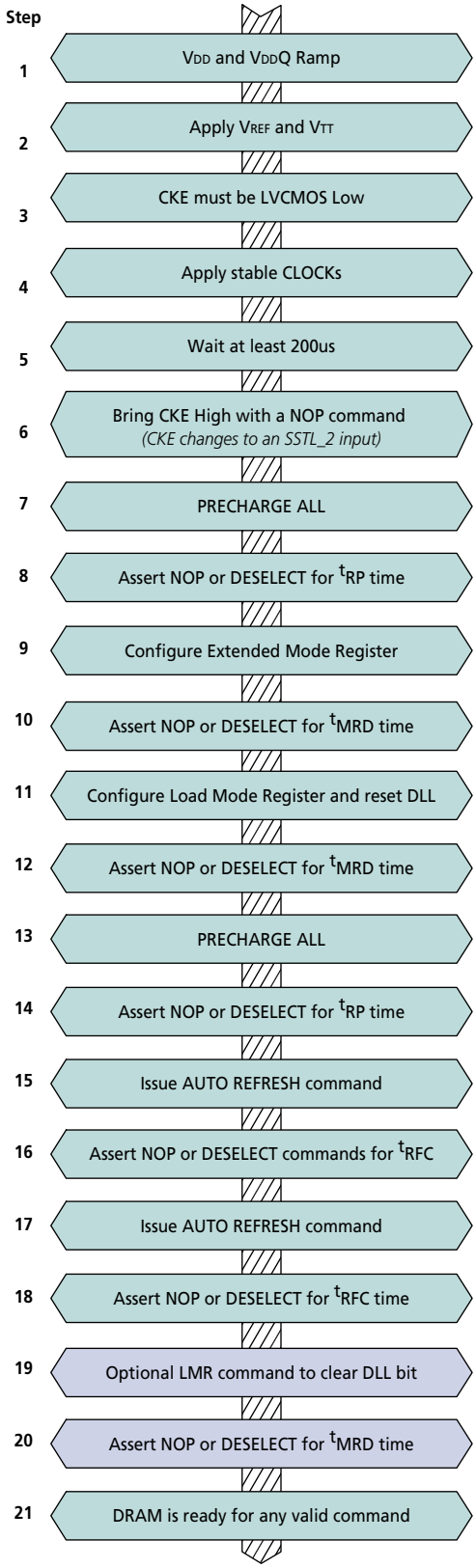
Step 20

Provide NOPs or DESELECT commands for at least ^{t}MRD.

Step 21

The DRAM has been properly initialized and is ready for any valid command. Note, 200 clock cycles are required between the DLL reset at Step 11 and any READ command.

Figure 1: Initialization Flow Diagram



Configuration of Operating Parameters

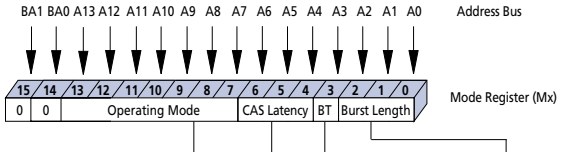
As part of the initialization routine the device operating parameters must be set. For standard DDR-1 SDRAM this includes two internal registers, the Mode Register (MR) and the Extended Mode Register (EMR).

The LOAD MODE REGISTER command (LMR) is used to program the mode registers. The LMR command is issued in conjunction with the DRAM bank addresses (BA1 and BA0), selects either the MR or the EMR. The DRAM row addresses (A13–A0) provide the op-code to be written. The least significant row address corresponds to the least significant bit within the mode registers.

Mode Register

The mode register has seven configurable bits that may be dynamically updated to reflect changing system requirements. They include (M0-M2) which are used to set the burst length, (M3) which is used to set the burst type, (M4-M6) which define the CAS Latency and (M8) which is used to perform a DLL reset. All other bits are reserved for future use and must be set to zero. To address the mode register, set BA1 = 0 and BA0 = 0.

Figure 2: Mode Register



M3	Burst Type
0	Sequential
1	Interleaved

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (DDR400 only)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

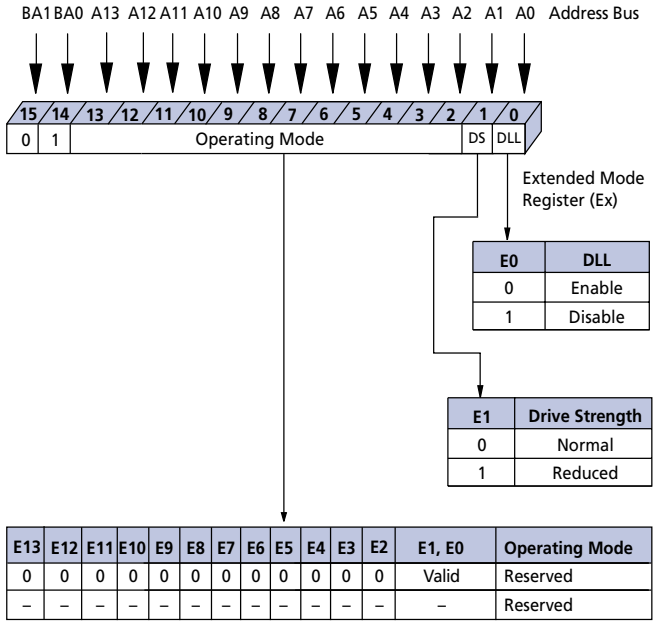
M13	M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	-	All other states reserved

Note:
1) BA1 and BA0 must be "0, 0" to select the mode register (vs. the extended mode register).
2) A13 is only utilized on the 1Gb device.
3) A12 is only utilized on 256Mb and larger devices.

Extended Mode Register

The EMR has two configurable bits that usually are not changed once the device has been initialized. Bit (E0) is used to enable the device DLL and bit (E2) defines the output drive strength. All other bits are reserved for future use and must be set to zero. To point to the EMR, set BA1 = 0 and BA0 =1.

Figure 3: Extended Mode Register



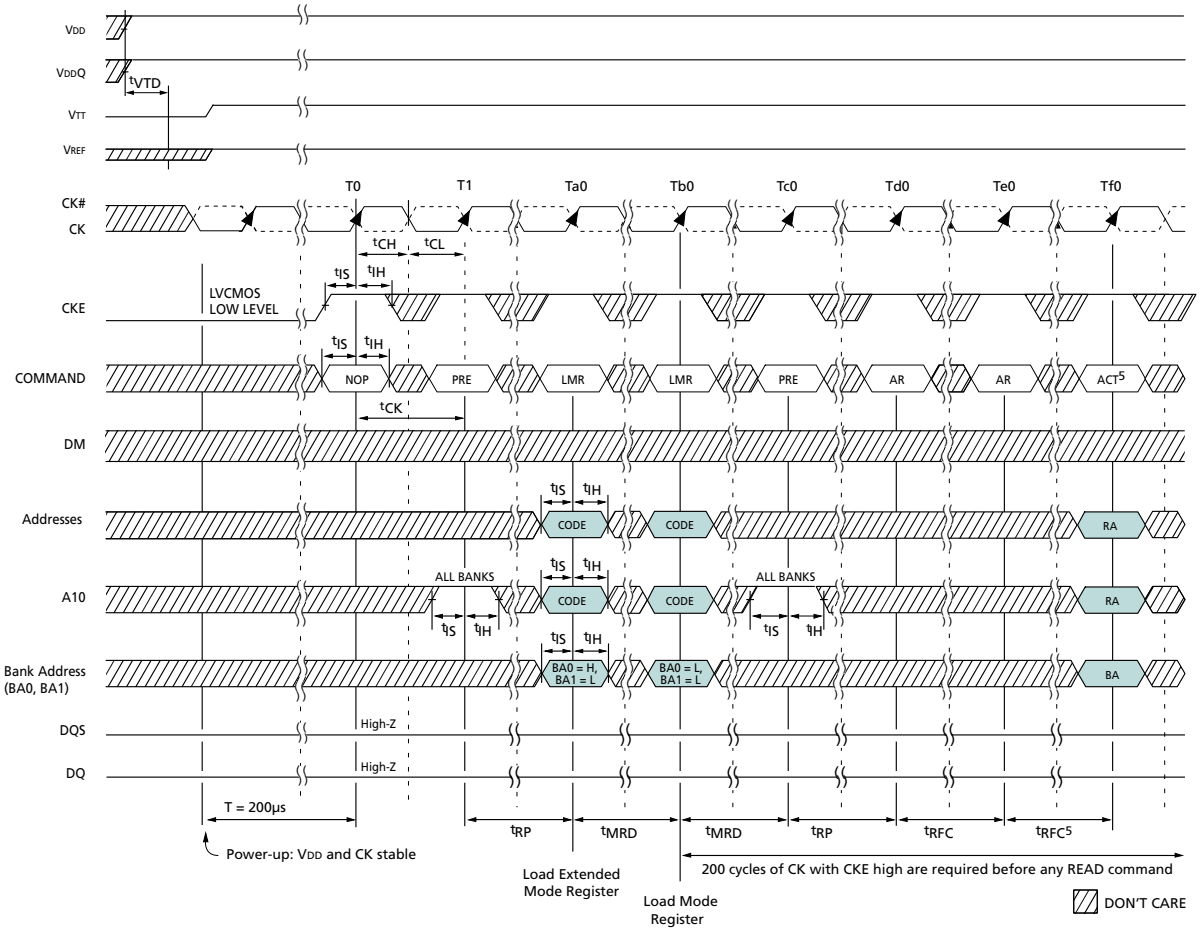
E0	DLL
0	Enable
1	Disable

E1	Drive Strength
0	Normal
1	Reduced

E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	–	–	Reserved

Note:
1) To access the extended mode register BA1 must equal "0" and BA0 must equal a "1".
2) A13 is only utilized on the 1Gb device.
3) A12 is only utilized on 256Mb and larger devices.
4) Reduced drive strength is avaliable on x16 devices only.

Figure 4: Initialization Waveform Sequence



Summary

The correct DRAM initialization sequence must be followed whenever the device is first powered up or any time there is an interruption in device power. Failure to follow documented procedures will jeopardize device functionality. The steps in this technical note provide a general flow for proper initialization; for exact device timing or device voltage levels, refer to the DDR component data sheet(s). For the latest data sheets, please refer to Micron's Web site at www.micron.com/datasheets.

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