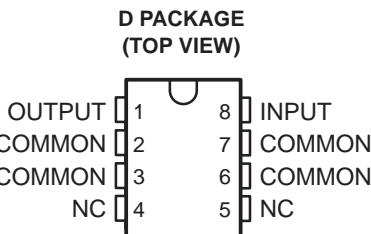


- 3-Terminal Regulators
- Output Current Up To 100 mA
- No External Components
- Internal Thermal-Overload Protection
- Internal Short-Circuit Current Limiting

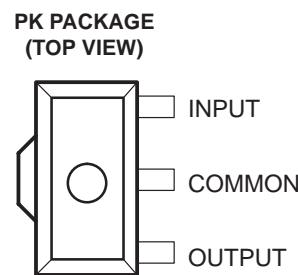
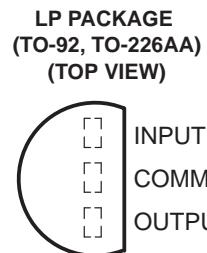
description/ordering information

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal-shutdown features of these regulators essentially make them immune to overload. When used as a replacement for a Zener diode-resistor combination, an effective improvement in output impedance can be obtained, together with lower bias current.

The µA78L00C and µA78L00AC series are characterized for operation over the virtual junction temperature range of 0°C to 125°C. The µA78L05AI is characterized for operation over the virtual junction temperature range of -40°C to 125°C.



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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μ A78L00 SERIES POSITIVE-VOLTAGE REGULATORS

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description/ordering information (continued)

ORDERING INFORMATION

T _J	V _{O(NOM)} (V)	OUTPUT VOLTAGE TOLERANCE	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	2.6 V	5%	SOIC (D)	Tube of 75	μ A78L02ACD	78L02A
			TO-226/TO-92 (LP)	Bulk of 1000	μ A78L02ACLP	78L02AC
	5 V	5%	SOIC (D)	Tube of 75	μ A78L05ACD	78L05A
				Reel of 2500	μ A78L05ACDR	
			TO-226/TO-92 (LP)	Bulk of 1000	μ A78L05ACLP	78L05AC
				Pack of 2000	μ A78L05ACLPM	
				Reel of 2000	μ A78L05ACLPR	
		10%	SOT-89 (PK)	Reel of 1000	μ A78L05ACPK	F5
			SOIC (D)	Tube of 75	μ A78L05CD	78L05C
				Reel of 2500	μ A78L05CDR	
			TO-92 (LP) TO-226AA (LP)	Bulk of 1000	μ A78L05CLP	78L05C
				Reel of 2000	μ A78L05CLPR	
			SOT-89 (PK)	Tube of	μ A78L05CPK	B5
	6.2 V	5%	TO-226/TO-92 (LP)	Bulk of 1000	μ A78L06ACLP	78L06AC
				Reel of 2000	μ A78L06ACLPR	
			SOT-89 (PK)	Reel of 1000	μ A78L06ACPK	F6
	8 V	5%	SOIC (D)	Tube of 75	μ A78L08ACD	78L08A
				Reel of 2500	μ A78L08ACDR	
			TO-226/TO-92 (LP)	Bulk of 1000	μ A78L08ACLP	78L08AC
				Reel of 2000	μ A78L08ACLPR	
			SOT-89 (PK)	Reel of 1000	μ A78L08ACPK	F8
			SOIC (D)	Tube of 75	μ A78L08CD	78L08C
				Reel of 2500	μ A78L08CDR	
	9 V	5%	SOIC (D)	Tube of 75	μ A78L09ACD	78L09A
				Reel of 2500	μ A78L09ACDR	
			TO-226/TO-92 (LP)	Bulk of 1000	μ A78L09ACLP	78L09AC
				Reel of 2000	μ A78L09ACLPR	
			SOT-89 (PK)	Reel of 1000	μ A78L09ACPK	F9
	10 V	5%	SOIC (D)	Tube of 75	μ A78L10ACD	78L10A
				Reel of 2500	μ A78L10ACDR	
			TO-226/TO-92 (LP)	Bulk of 1000	μ A78L10ACLP	78L10AC
				Reel of 2000	μ A78L10ACLPR	
			SOT-89 (PK)	Reel of 1000	μ A78L10ACPK	FA
	12 V	5%	SOIC (D)	Tube of 75	μ A78L12ACD	78L12A
				Reel of 2500	μ A78L12ACDR	
			TO-226/TO-92 (LP)	Bulk of 1000	μ A78L12ACLP	78L12AC
				Pack of 2000	μ A78L12ACLPM	
				Reel of 2000	μ A78L12ACLPR	
			SOT-89 (PK)	Reel of 1000	μ A78L12ACPK	FC

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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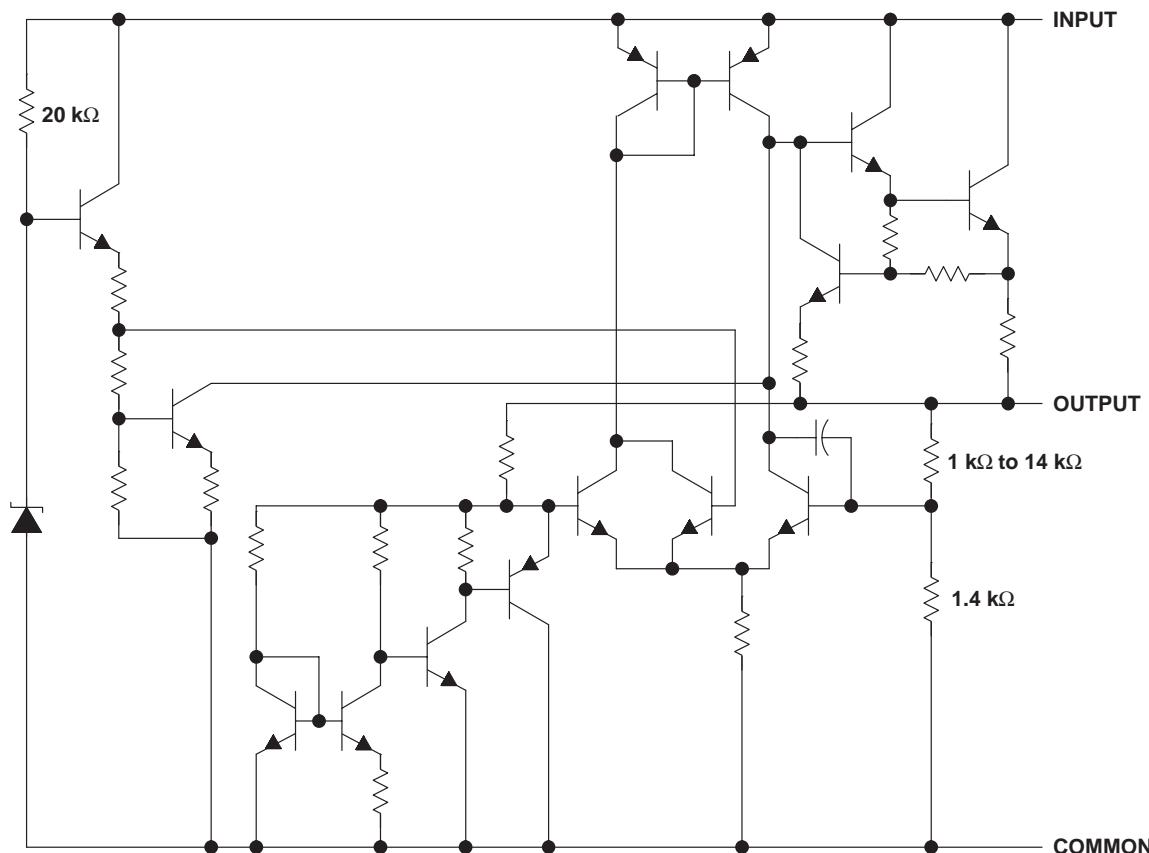
description/ordering information (continued)

ORDERING INFORMATION (continued)

T _J	V _{O(NOM)} (V)	OUTPUT VOLTAGE TOLERANCE	PACKAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	15 V	5%	SOIC (D)	Tube of 75 µA78L15ACD	78L15A
				Reel of 2500 µA78L15ACDR	
			TO-226/TO-92 (LP)	Bulk of 1000 µA78L15ACLP	78L15AC
				Reel of 2000 µA78L15ACLPR	
-40°C to 125°C	5 V	5%	SOT-89 (PK)	Reel of 1000 µA78L15ACPK	FF
			TO-226/TO-92 (LP)	Bulk of 1000 µA78L05AILP	78L05AI
				Reel of 2000 µA78L05AILPR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic



NOTE A: Resistor values shown are nominal.

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absolute maximum ratings over virtual junction temperature range (unless otherwise noted)[†]

Input voltage, V_I : μA78L02AC, μA78L05C–μA78L09C, μA78L10AC	30 V
μA78L12C, μA78L12AC, μA78L15C, μA78L15AC	35 V
Virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

package thermal data (see Note 1)

PACKAGE	BOARD	θ_{JC}	θ_{JA}
SOIC (D)	High K, JESD 51-7	39°C/W	97°C/W
TO-92/TO-226AA (LP)	High K, JESD 51-7	55°C/W	140°C/W
SOT-89 (PK)	High K, JESD 51-7	9°C/W	52°C/W

NOTE 1: Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal-overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
V_I Input voltage	μA78L02AC	4.75	20	V
	μA78L05C, μA78L05AC	7	20	
	μA78L06C, μA78L06AC	8.5	20	
	μA78L08C, μA78L08AC	10.5	23	
	μA78L09C, μA78L09AC	11.5	24	
	μA78L10AC	12.5	25	
	μA78L12C, μA78L12AC	14.5	27	
	μA78L15C, μA78L15AC	17.5	30	
I_O	Output current	100	mA
T_J	Operating virtual junction temperature range	μA78LxxC and μA78LxxAC series	0	125
		μA78L05AI	-40	125

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electrical characteristics at specified virtual junction temperature, $V_I = 9 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J^\dagger	$\mu\text{A78L02AC}$			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 4.75 \text{ V to } 20 \text{ V}$, $I_O = 1 \text{ mA to } 40 \text{ mA}$	25°C	2.5	2.6	2.7	V
		0°C to 125°C	2.45		2.75	
	$I_O = 1 \text{ mA to } 70 \text{ mA}$	0°C to 125°C	2.45		2.75	
Input voltage regulation	$V_I = 4.75 \text{ V to } 20 \text{ V}$	25°C		20	100	mV
	$V_I = 5 \text{ V to } 20 \text{ V}$			16	75	
Ripple rejection	$V_I = 6 \text{ V to } 20 \text{ V}$, $f = 120 \text{ Hz}$	25°C	43	51		dB
Output voltage regulation	$I_O = 1 \text{ mA to } 100 \text{ mA}$	25°C		12	50	mV
	$I_O = 1 \text{ mA to } 40 \text{ mA}$			6	25	
Output noise voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}$	25°C		30		µV
Dropout voltage		25°C		1.7		V
Bias current		25°C		3.6	6	mA
					5.5	
Bias current change	$V_I = 5 \text{ V to } 20 \text{ V}$	0°C to 125°C			2.5	mA
	$I_O = 1 \text{ mA to } 40 \text{ mA}$				0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 10 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J^\dagger	$\mu\text{A78L05C}$			$\mu\text{A78L05AC}$ $\mu\text{A78L05AI}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 7 \text{ V to } 20 \text{ V}$, $I_O = 1 \text{ mA to } 40 \text{ mA}$	25°C	4.6	5	5.4	4.8	5	5.2	V
		Full range	4.5		5.5	4.75		5.25	
	$I_O = 1 \text{ mA to } 70 \text{ mA}$	Full range	4.5		5.5	4.75		5.25	
Input voltage regulation	$V_I = 7 \text{ V to } 20 \text{ V}$	25°C		32	200	32	150		mV
	$V_I = 8 \text{ V to } 20 \text{ V}$			26	150	26	100		
Ripple rejection	$V_I = 8 \text{ V to } 18 \text{ V}$, $f = 120 \text{ Hz}$	25°C	40	49		41	49		dB
Output voltage regulation	$I_O = 1 \text{ mA to } 100 \text{ mA}$	25°C		15	60	15	60		mV
	$I_O = 1 \text{ mA to } 40 \text{ mA}$			8	30	8	30		
Output noise voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}$	25°C		42		42			µV
Dropout voltage		25°C		1.7		1.7			V
Bias current		25°C		3.8	6	3.8	6		mA
					5.5		5.5		
Bias current change	$V_I = 8 \text{ V to } 20 \text{ V}$	Full range			1.5		1.5		mA
	$I_O = 1 \text{ mA to } 40 \text{ mA}$				0.2		0.1		

‡ Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output. Full range for the µA78L05AC is $T_J = 0^\circ\text{C to } 125^\circ\text{C}$, and full range for the µA78L05AI is $T_J = -40^\circ\text{C to } 125^\circ\text{C}$.

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electrical characteristics at specified virtual junction temperature, $V_I = 12 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J^\dagger	μ A78L06C			μ A78L06AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 8.5 \text{ V to } 20 \text{ V}$, $I_O = 1 \text{ mA to } 40 \text{ mA}$	25°C	5.7	6.2	6.7	5.95	6.2	6.45	V
		0°C to 125°C	5.6	6.8		5.9		6.5	
	$I_O = 1 \text{ mA to } 70 \text{ mA}$	0°C to 125°C	5.6	6.8		5.9		6.5	
Input voltage regulation	$V_I = 8.5 \text{ V to } 20 \text{ V}$	25°C		35	200		35	175	mV
	$V_I = 9 \text{ V to } 20 \text{ V}$			29	150		29	125	
Ripple rejection	$V_I = 10 \text{ V to } 20 \text{ V}$, $f = 120 \text{ Hz}$	25°C	39	48		40	48		dB
Output voltage regulation	$I_O = 1 \text{ mA to } 100 \text{ mA}$	25°C		16	80		16	80	mV
	$I_O = 1 \text{ mA to } 40 \text{ mA}$			9	40		9	40	
Output noise voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}$	25°C		46			46		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.9	6		3.9	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 9 \text{ V to } 20 \text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1 \text{ mA to } 40 \text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μF capacitor across the input and a 0.1- μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 14 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J^\dagger	μ A78L08C			μ A78L08AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 10.5 \text{ V to } 23 \text{ V}$, $I_O = 1 \text{ mA to } 40 \text{ mA}$	25°C	7.36	8	8.64	7.7	8	8.3	V
		0°C to 125°C	7.2		8.8	7.6		8.4	
	$I_O = 1 \text{ mA to } 70 \text{ mA}$	0°C to 125°C	7.2		8.8	7.6		8.4	
Input voltage regulation	$V_I = 10.5 \text{ V to } 23 \text{ V}$	25°C		42	200		42	175	mV
	$V_I = 11 \text{ V to } 23 \text{ V}$			36	150		36	125	
Ripple rejection	$V_I = 13 \text{ V to } 23 \text{ V}$, $f = 120 \text{ Hz}$	25°C	36	46		37	46		dB
Output voltage regulation	$I_O = 1 \text{ mA to } 100 \text{ mA}$	25°C		18	80		18	80	mV
	$I_O = 1 \text{ mA to } 40 \text{ mA}$			10	40		10	40	
Output noise voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}$	25°C		54			54		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4	6		4	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 11 \text{ V to } 23 \text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1 \text{ mA to } 40 \text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μF capacitor across the input and a 0.1- μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 16 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J^\dagger	µA78L09C			µA78L09AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 12 \text{ V}$ to 24 V , $I_O = 1 \text{ mA}$ to 40 mA	25°C	8.3	9	9.7	8.6	9	9.4	V
		0°C to 125°C	8.1		9.9	8.55		9.45	
	$I_O = 1 \text{ mA}$ to 70 mA	0°C to 125°C	8.1		9.9	8.55		9.45	
Input voltage regulation	$V_I = 12 \text{ V}$ to 24 V	25°C		45	225		45	175	mV
	$V_I = 13 \text{ V}$ to 24 V			40	175		40	125	
Ripple rejection	$V_I = 15 \text{ V}$ to 25 V , $f = 120 \text{ Hz}$	25°C	36	45		38	45		dB
Output voltage regulation	$I_O = 1 \text{ mA}$ to 100 mA	25°C		19	90		19	90	mV
	$I_O = 1 \text{ mA}$ to 40 mA			11	40		11	40	
Output noise voltage	$f = 10 \text{ Hz}$ to 100 kHz	25°C		58			58		µV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.1	6		4.1	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 13 \text{ V}$ to 24 V	0°C to 125°C			1.5			1.5	mA
	$I_O = 1 \text{ mA}$ to 40 mA				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.33\text{-}\mu\text{F}$ capacitor across the input and a $0.1\text{-}\mu\text{F}$ capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 14 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J^\dagger	µA78L10AC			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 13 \text{ V}$ to 25 V , $I_O = 1 \text{ mA}$ to 40 mA	25°C	9.6	10	10.4	V
		0°C to 125°C	9.5		10.5	
	$I_O = 1 \text{ mA}$ to 70 mA	0°C to 125°C	9.5		10.5	
Input voltage regulation	$V_I = 13 \text{ V}$ to 25 V	25°C		51	175	mV
	$V_I = 14 \text{ V}$ to 25 V			42	125	
Ripple rejection	$V_I = 15 \text{ V}$ to 25 V , $f = 120 \text{ Hz}$	25°C	37	44		dB
Output voltage regulation	$I_O = 1 \text{ mA}$ to 100 mA	25°C		20	90	mV
	$I_O = 1 \text{ mA}$ to 40 mA			11	40	
Output noise voltage	$f = 10 \text{ Hz}$ to 100 kHz	25°C		62		µV
Dropout voltage		25°C		1.7		V
Bias current		25°C		4.2	6	mA
		125°C			5.5	
Bias current change	$V_I = 14 \text{ V}$ to 25 V	0°C to 125°C			1.5	mA
	$I_O = 1 \text{ mA}$ to 40 mA				0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.33\text{-}\mu\text{F}$ capacitor across the input and a $0.1\text{-}\mu\text{F}$ capacitor across the output.

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electrical characteristics at specified virtual junction temperature, $V_I = 19 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J^\dagger	μ A78L12C			μ A78L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 14 \text{ V to } 27 \text{ V}$, $I_O = 1 \text{ mA to } 40 \text{ mA}$	25°C	11.1	12	12.9	11.5	12	12.5	V
		0°C to 125°C	10.8		13.2	11.4		12.6	
	$I_O = 1 \text{ mA to } 70 \text{ mA}$	0°C to 125°C	10.8		13.2	11.4		12.6	
Input voltage regulation	$V_I = 14.5 \text{ V to } 27 \text{ V}$	25°C		55	250		55	250	mV
	$V_I = 16 \text{ V to } 27 \text{ V}$			49	200		49	200	
Ripple rejection	$V_I = 15 \text{ V to } 25 \text{ V}$, $f = 120 \text{ Hz}$	25°C	36	42		37	42		dB
Output voltage regulation	$I_O = 1 \text{ mA to } 100 \text{ mA}$	25°C		22	100		22	100	mV
	$I_O = 1 \text{ mA to } 40 \text{ mA}$			13	50		13	50	
Output noise voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}$	25°C		70			70		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.3	6.5		4.3	6.5	mA
		125°C		6			6		
Bias current change	$V_I = 16 \text{ V to } 27 \text{ V}$	0°C to 125°C		1.5			1.5		mA
	$I_O = 1 \text{ mA to } 40 \text{ mA}$			0.2			0.1		

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μF capacitor across the input and a 0.1- μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 23 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J^\dagger	μ A78L15C			μ A78L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 17.5 \text{ V to } 30 \text{ V}$, $I_O = 1 \text{ mA to } 40 \text{ mA}$	25°C	13.8	15	16.2	14.4	15	15.6	V
		0°C to 125°C	13.5		16.5	14.25		15.75	
	$I_O = 1 \text{ mA to } 70 \text{ mA}$	0°C to 125°C	13.5		16.5	14.25		15.75	
Input voltage regulation	$V_I = 17.5 \text{ V to } 30 \text{ V}$	25°C		65	300		65	300	mV
	$V_I = 20 \text{ V to } 30 \text{ V}$			58	250		58	250	
Ripple rejection	$V_I = 18.5 \text{ V to } 28.5 \text{ V}$, $f = 120 \text{ Hz}$	25°C	33	39		34	39		dB
Output voltage regulation	$I_O = 1 \text{ mA to } 100 \text{ mA}$	25°C		25	150		25	150	mV
	$I_O = 1 \text{ mA to } 40 \text{ mA}$			15	75		15	75	
Output noise voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}$	25°C		82			82		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.6	6.5		4.6	6.5	mA
		125°C		6			6		
Bias current change	$V_I = 10 \text{ V to } 30 \text{ V}$	0°C to 125°C		1.5			1.5		mA
	$I_O = 1 \text{ mA to } 40 \text{ mA}$			0.2			0.1		

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μF capacitor across the input and a 0.1- μF capacitor across the output.



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APPLICATION INFORMATION

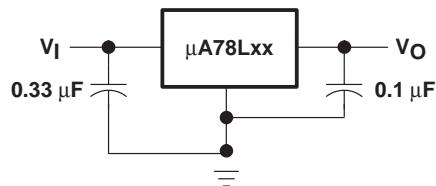


Figure 1. Fixed-Output Regulator

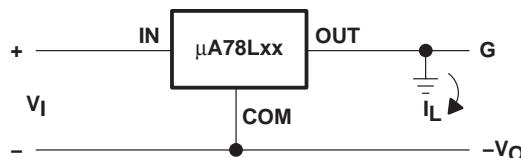


Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)

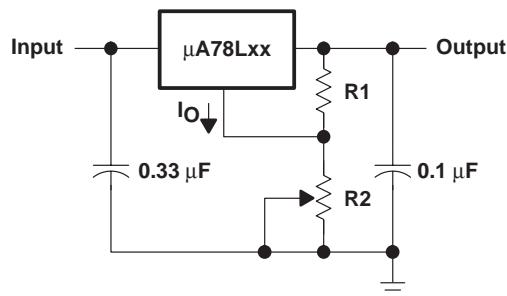


Figure 3. Adjustable-Output Regulator

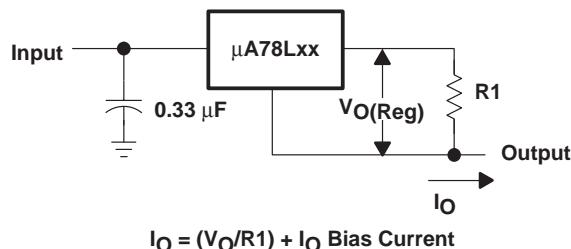


Figure 4. Current Regulator

μ A78L00 SERIES POSITIVE-VOLTAGE REGULATORS

SLVS010R – JANUARY 1976 – REVISED OCTOBER 2003

APPLICATION INFORMATION

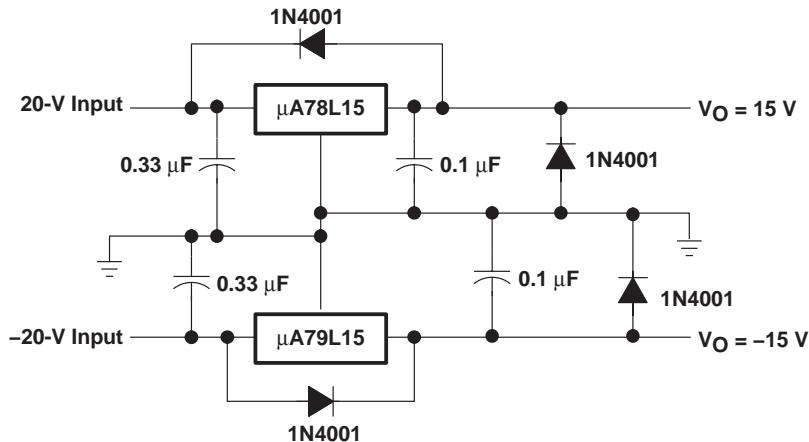


Figure 5. Regulated Dual Supply

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

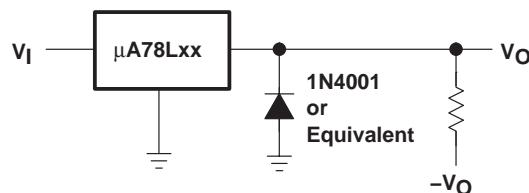


Figure 6. Output Polarity-Reversal-Protection Circuit

reverse-bias protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This can occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series-pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed as shown in Figure 7.

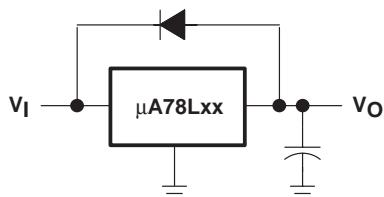
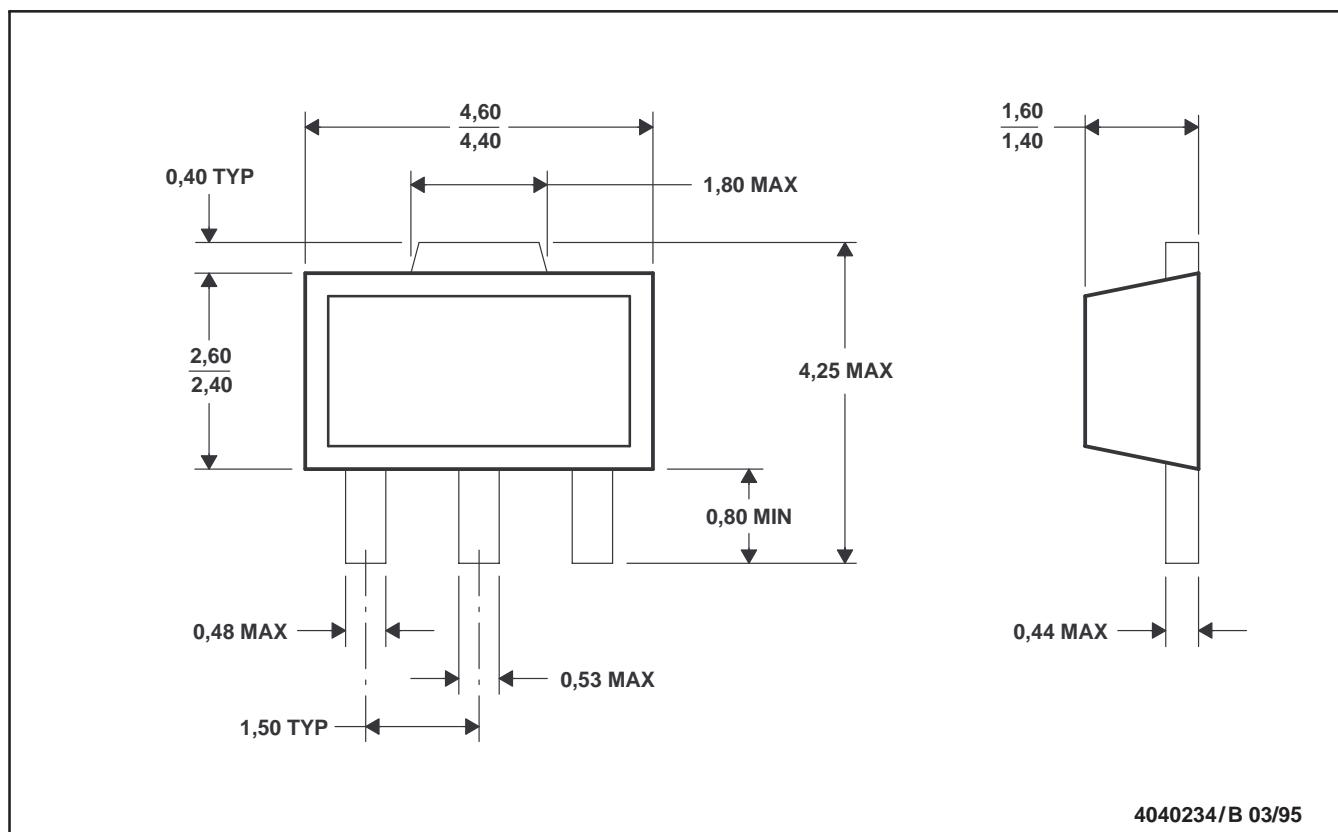


Figure 7. Reverse-Bias-Protection Circuit

PK (R-PSSO-F3)

PLASTIC SINGLE-IN-LINE PACKAGE

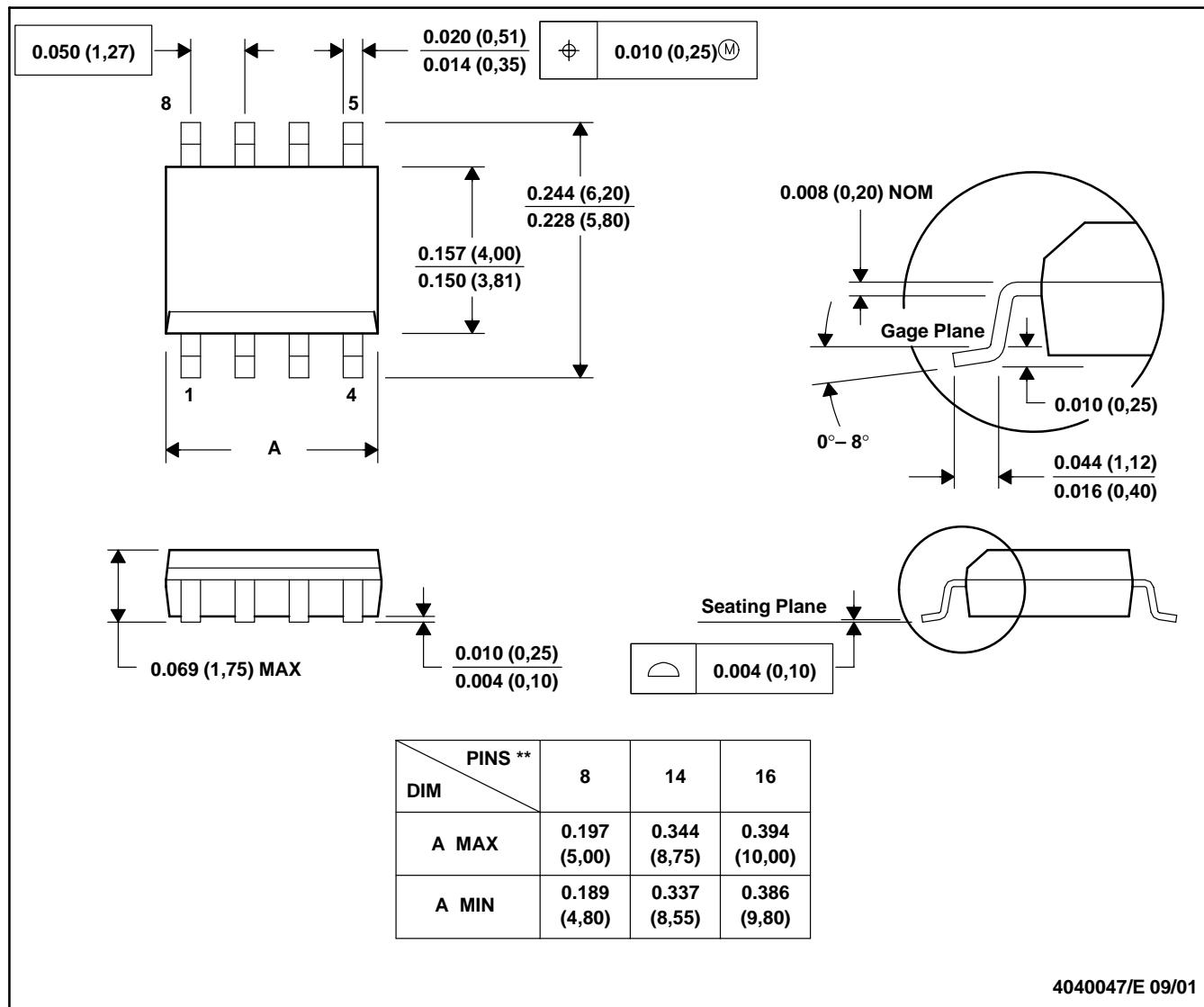


- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

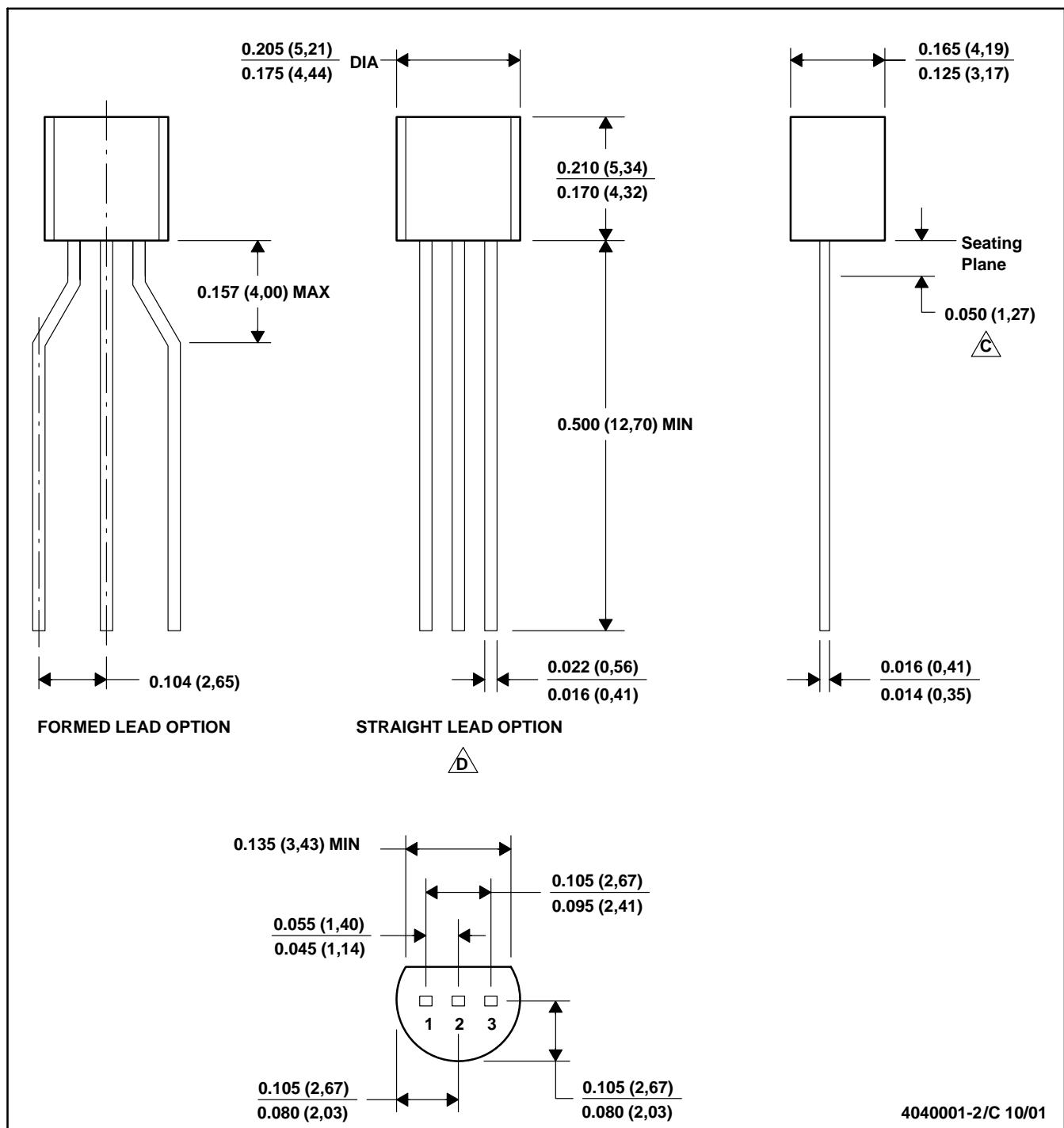


4040047/E 09/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0.15).
 D. Falls within JEDEC MS-012

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Lead dimensions are not controlled within this area

D. Falls within JEDEC TO -226 Variation AA (TO-226 replaces TO-92)

E. Shipping Method:

Straight lead option available in bulk pack only.

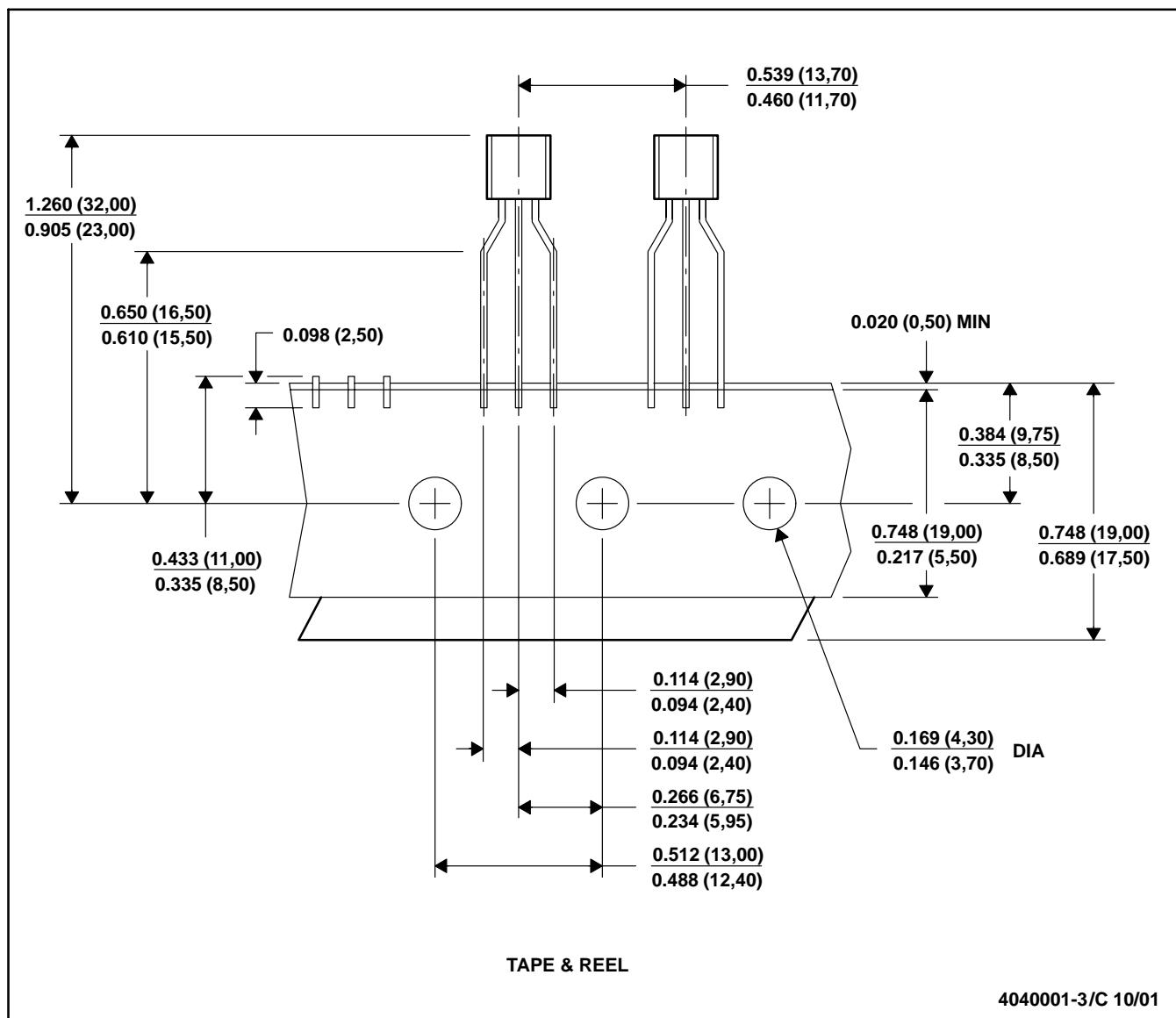
Formed lead option available in tape & reel or ammo pack.

MECHANICAL DATA

MSOT002A – OCTOBER 1994 – REVISED NOVEMBER 2001

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Format Lead Option package.

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