

MC10H125

Quad MECL-to-TTL Translator

The MC10H125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

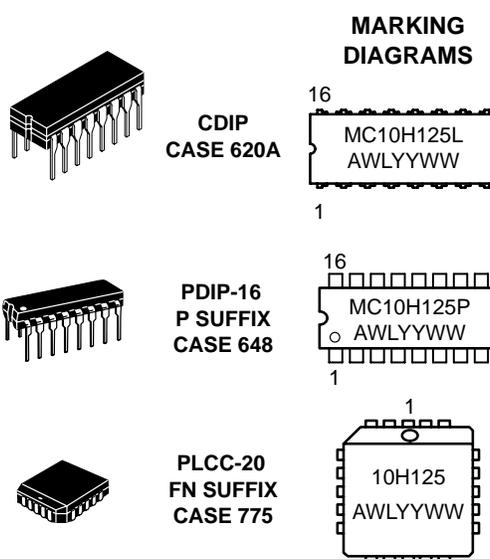
Outputs of unused translators will go to low state when their inputs are left open.

- Propagation Delay, 2.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV
(Over Operating Voltage and Temperature Range)
- MECL 10K-Compatible



ON Semiconductor®

<http://onsemi.com>



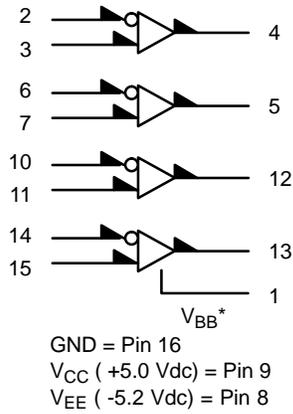
A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H125L	CDIP	25 Units/Rail
MC10H125P	PDIP-16	25 Units/Rail
MC10H125FN	PLCC-20	46 Units/Rail

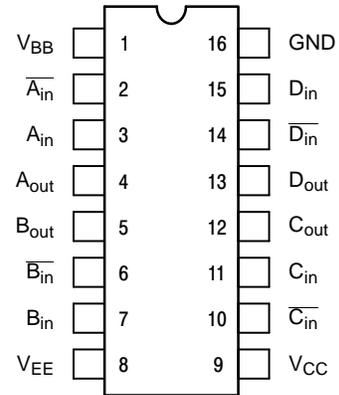
MC10H125

LOGIC DIAGRAM



* V_{BB} to be used to supply bias to the MC10H125 only and bypassed (when used) with 0.01 μ F to 0.1 μ F capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

DIP CONVERSION TABLES

16-Pin DIL to 20-Pin PLCC

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20-Pin DIL to 20-Pin PLCC

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

MC10H125

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit	
V _{EE}	Power Supply (V _{CC} = 5.0 V)	-8.0 to 0	Vdc	
V _{CC}	Power Supply (V _{EE} = -5.2 V)	0 to +7.0	Vdc	
V _I	Input Voltage (V _{CC} = 5.0 V)	0 to V _{EE}	Vdc	
T _A	Operating Temperature Range	0 to +75	°C	
T _{stg}	Storage Temperature Range	- Plastic - Ceramic	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V +5%; V_{CC} = 5.0 V + 5.0 %) (Note 2)

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
I _E	Negative Power Supply Drain Current	-	44	-	40	-	44	mA
I _{CCH}	Positive Power Supply Drain Current	-	63	-	63	-	63	mA
I _{CCL}		-	40	-	40	-	40	mA
I _{inH}	Input Current	-	225	-	145	-	145	μA
I _{CBO}	Input Leakage Current	-	1.5	-	1.0	-	1.0	μA
V _{OH}	High Output Voltage I _{OH} = -1.0 mA	2.5	-	2.5	-	2.5	-	Vdc
V _{OL}	Low Output Voltage I _{OL} = +20 mA	-	0.5	-	0.5	-	0.5	Vdc
V _{IH}	High Input Voltage (Note 1)	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V _{IL}	Low Input Voltage (Note 1)	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
I _{OS}	Short Circuit Current	60	150	60	150	50	150	mA
V _{BB}	Reference Voltage	-1.38	-1.27	-1.35	-1.25	-1.31	-1.19	Vdc
V _{CMR}	Common Mode Range (Note 3)	-	-	-2.85 to +0.3				V
Typical								
V _{PP}	Input Sensitivity (Note 4)	150						mV

AC PARAMETERS

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
t _{pd}	Propagation Delay	0.8	3.3	0.85	3.35	0.9	3.4	ns
t _r	Rise Time (Note 5)	0.3	1.2	0.3	1.2	0.3	1.2	ns
t _f	Fall Time (Note 5)	0.3	1.2	0.3	1.2	0.3	1.2	ns

1. When V_{BB} is used as the reference voltage.
2. Each MECL 10H series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
3. Differential input not to exceed 1.0 Vdc.
4. 150 mV_{p-p} differential input required to obtain full logic swing on output.
5. Output Voltage = 1.0 V to 2.0 V. R_L = 500 Ω to GND and C_L = 25 pF to GND. Refer to Figure 1.

MC10H125

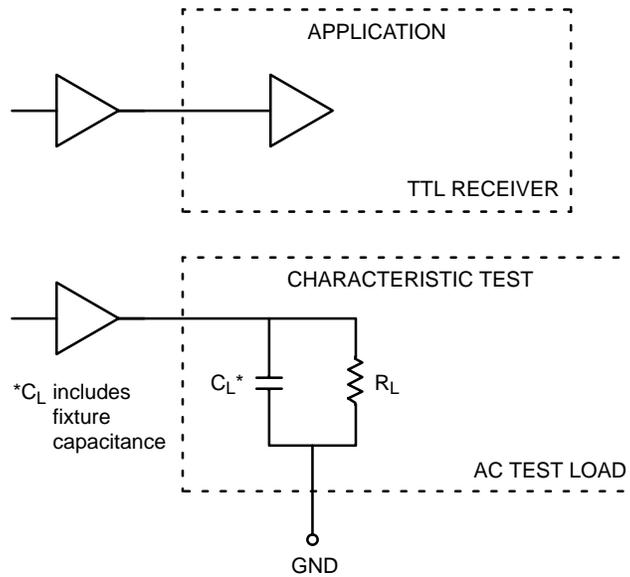


Figure 1. TTL Output Loading Used for Device Evaluation

APPLICATION INFORMATION

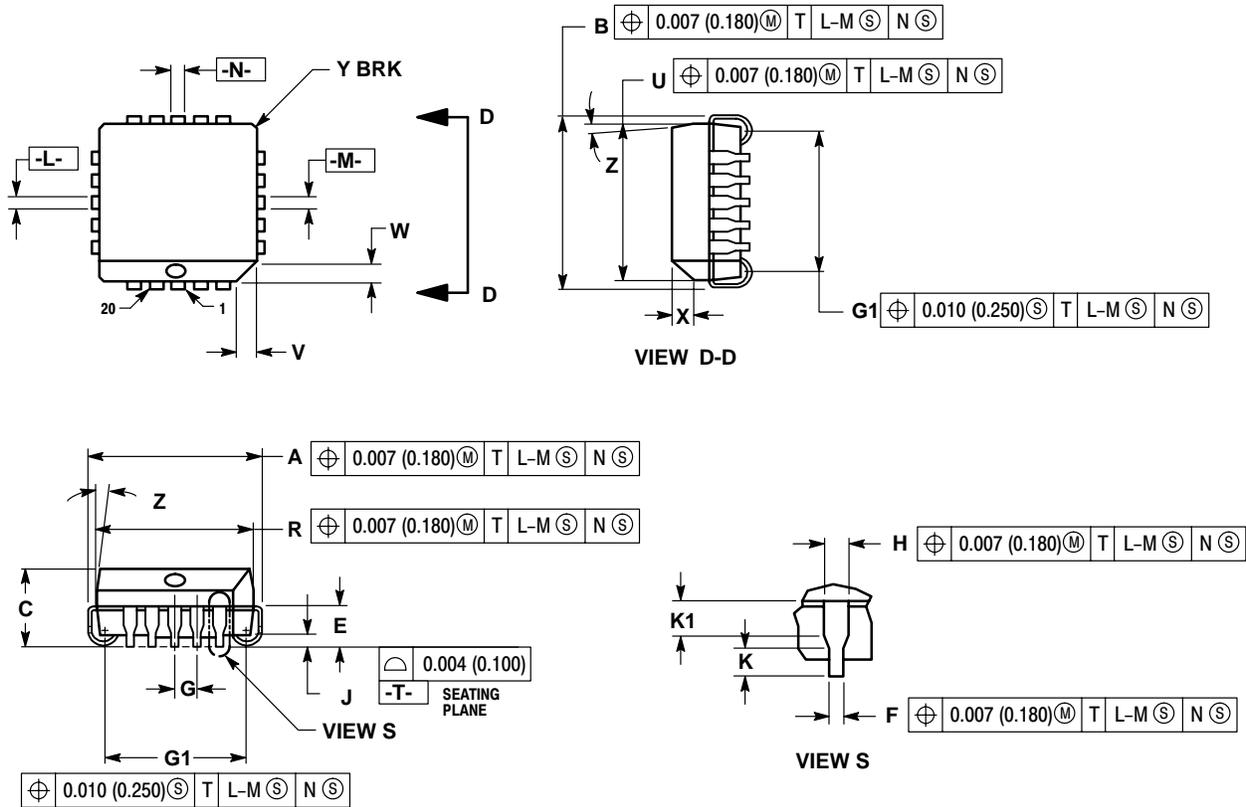
The MC10H125 incorporates differential inputs and Schottky TTL “totem pole” outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low-logic level whenever the inputs are left floating, and a high-logic output level is achieved with a minimum input level of 150 mV_{p-p} .

An advantage of this device is that MECL-level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and -5.2 volts.

MC10H125

PACKAGE DIMENSIONS

PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE D



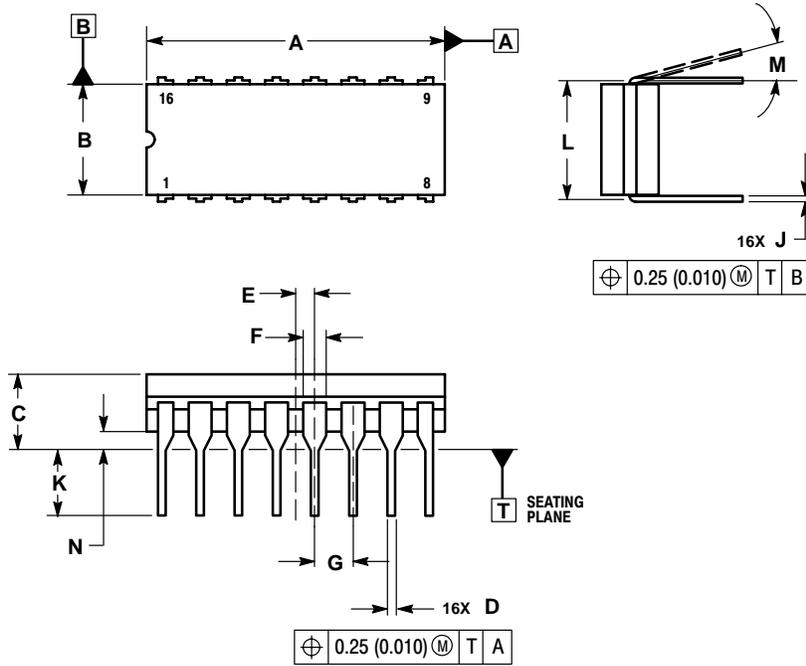
NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

MC10H125

CDIP
CASE 620A-01
ISSUE O



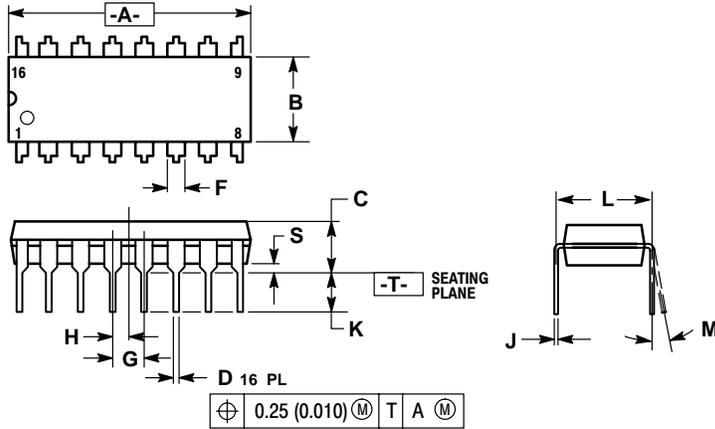
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620-10.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.01

MC10H125

PDIP-16
P SUFFIX
 PLASTIC DIP PACKAGE
 CASE 648-08
 ISSUE R



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

STYLE 1:

- PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. CATHODE
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 15. ANODE
 16. ANODE

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