

Overview

This document presents all circuits on the Digilab XL board, and discusses how to use and program the on-board FPGA. Further pertinent information can be found in other documents, some of which are listed below.

To learn...	Consult this document...	Located on the...
How to test the Digilab XL board	Digilab XL test procedure	Digilab XL web page
About the Digilab XL parts list	Digilab Standard BOM	Digilab XL web page
About Digilab's components	Digilab components tutorial	Tutorial page
About Digilab assembly	Digilab assembly tutorial	Tutorial page
About soldering techniques	Soldering tutorial	Tutorial page
About breadboarding circuits	Breadboard tutorial	Tutorial page
The FPGA pin definitions	Digilab XL FPGA Pinlist	Digilab XL web page

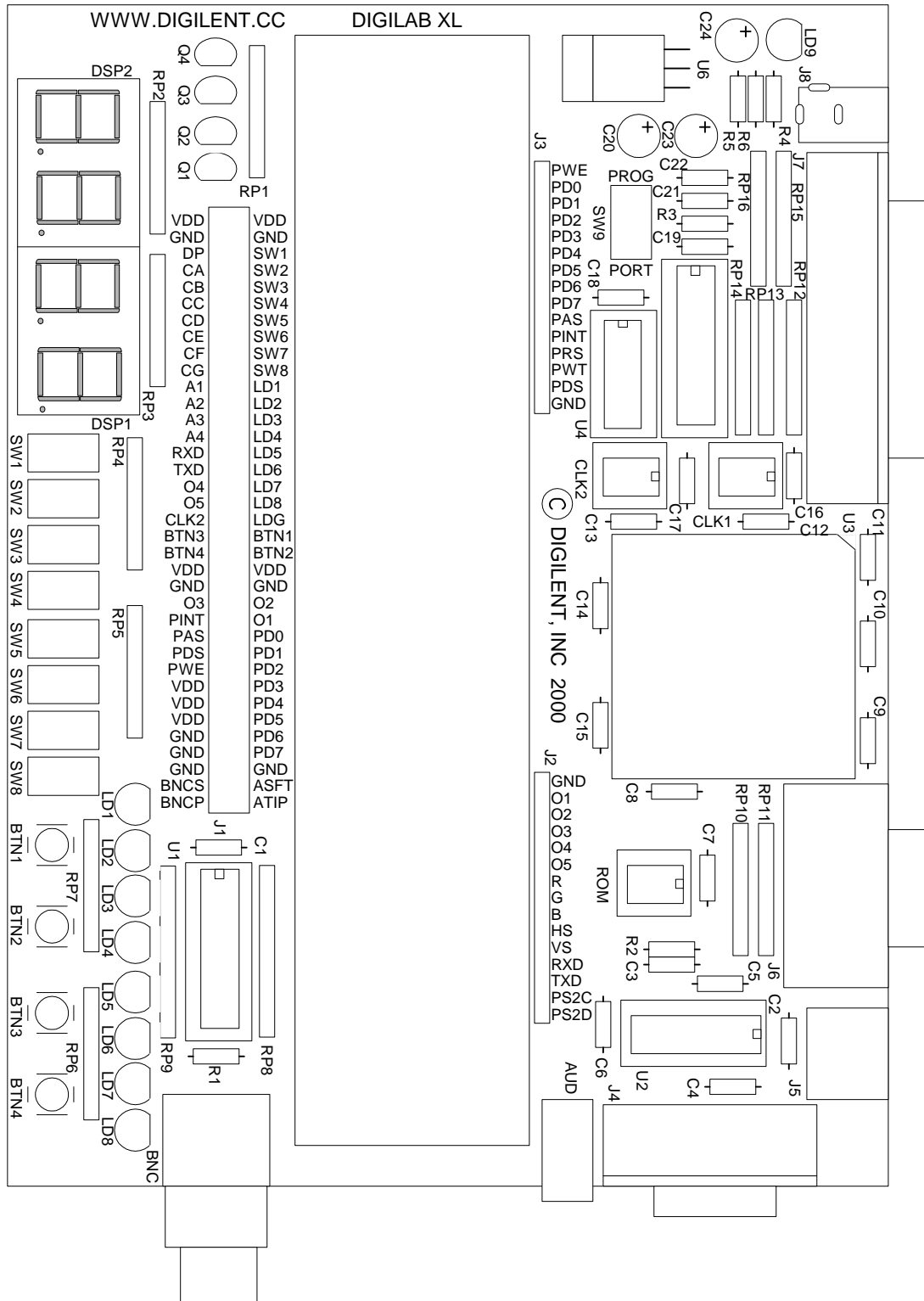
This document presents information on the following topics.

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Parts List

Item	Qty	Description	Reference Designator
1	1	Stereo audio jack 1/8"	AUD
2	1	Right angle BNC, PCB mount	BNC
3	4	Momentary contact push button	BTN1-BTN4
4	19	Axial ceramic .1uF cap	C1-19
5	1	1.5uF 25V dipped tantalum	C24
6	2	10uF 6.3V dipped tantalum	C20, C23
7	2	33pF ceramic cap	C21, C22
8	1	25.175MHz CMOS oscillator. 1/2 size	CLK1 (socketed)
9	2	7-seg LED display, .56, CA, 2 digit	DSP1, DSP2
10	1	72 pin DIP socket (from 3M)	J1
11	1	15-pin header (use one 30 pin strip)	J2, J3
12	1	DB9 female serial port connector	J4
13	1	6 pin mini-din PS/2 connector	J5
14	1	DB15 3-row VGA connector	J6
15	1	DB25 parallel port female connector	J7
16	1	2.1mm power connector	J8
17	9	RED LEDs in T 1 3/4 package	LD1-LD9
18	4	2N3904 transistors in TO-92 package	Q1-Q4
19	1	1/4W resistor 10K (1/8W OK)	R1
20	2	1/4W resistor 1K (1/8W OK)	R2,R3
21	2	1/4W resistor 240 (1/8W OK)	R4, R5
22	1	1/4W resistor 750 (1/8W OK)	R6
23	5	Isolated resistor pack 220 (8 pin)	RP1, 12, 13, 15, 16
24	2	Isolated resistor pack 100 (8 pin)	RP2, 3
25	6	Isolated resistor pack 4.7K (8 pin)	RP4, 5, 6, 7, 10, 14
26	1	Bussed resistor pack 10K (10 pin)	RP8
27	1	Bussed resistor pack 270 (10 pin)	RP9
28	1	Isolated resistor pack 470 (8 pin)	RP11
29	9	STDP slide switch	SW1-9
30	1	74HC373	U1 (socketed)
31	1	84 pin PLCC Spartan FPGA	U3 (socketed)
32	1	74HC125	U4 (socketed)
33	1	74ACT244	U5 (socketed)
34	1	LM317T in TO-220	U6
35	3	8-pin DIP socket	Socket CLK1 & 2, ROM
36	2	20-pin DIP socket	Socket U1, U5
37	1	16-pin DIP socket	Socket U2
38	1	84-pin PLCC socket	Socket U3
39	1	14-pin DIP socket	Socket U4
40	1	6.5" x 1.4" 630 tie point breadboard	NA
41	4	6/32 .250 hex standoff	NA
42	5	6/32 .250 machine screw	NA
43	1	6/32 standard nut	NA
44	1	Digilab raw PCB	NA

Board Graphic



Signals

The Digilab board has been designed to allow rapid circuit construction and convenient test lead attachment. Most signals are routed to the prototyping connector (J1), to the gate array, and to a test lead connector. Depending on function, the signals arise from devices or connectors on the board, or they drive devices or connectors on the board. The following table defines all Digilab signals and shows all their connections.

Signal	Definition	Connections
A1 - A4	Seven-segment Anode connections	SSDs, FPGA, J1
CA - CG	Seven-segment Cathode connections	SSDs, FPGA, J1
DP	Seven-segment Decimal Point connection	SSDs, J1
BTN1 - BTN4	Push Button connections	Buttons, FPGA, J1
SW1 - SW8	Slide switch connections	Switches, FPGA, J1
LD1 - LD8	LED connections	LEDs, FPGA, J1
LDG	Gate connection on LED driver 74HC373	74HC373, FPGA, J1
ASFT	Audio connector shaft	Audio connector, J1
ATIP	Audio connector tip	Audio connector, J1
CLK1	CLK1 connected to PGCK1 (pin 13)	CLK1, FPGA
CLK2	CLK2 connected to PGCK2 (pin 35)	CLK2, FPGA, J1
O1 - O5	User configurable (unassigned) FPGA pins	FPGA, J1, J2
PD0 - PD7	Parallel port data pins	J7 (par. port), FPGA, J1, J3
PWE	Parallel port Write Enable (EPP mode)	J7 (par. port), FPGA, J1, J3
PAS	Parallel port Address Strobe (EPP mode)	J7 (par. port), FPGA, J1, J3
PDS	Parallel port Data Strobe (EPP mode)	J7 (par. port), FPGA, J1, J3
PINT	Parallel port Interrupt (EPP mode)	J7 (par. port), FPGA, J1, J3
PRS	Parallel port Reset (EPP mode)	J7 (par. port), FPGA, J1, J3
PWT	Parallel port Wait/Busy (EPP mode)	J7 (par. port), FPGA, J3
BNCS	BNC connector shield	BNC connector, J1
BNCP	BNC connector center post	BNC connector, J1
R, G, B	VGA Red, Green, and Blue signals	J6 (vga connector), FPGA, J2
HS	VGA Horizontal Sync	J6 (vga connector), FPGA, J2
VS	VGA Vertical Sync	J6 (vga connector), FPGA, J2
RXD, TXD	RS-232 receive and send signals	J4 (serial connector), FPGA, J2
PS2D, PS2C	PS2 port data and clock signals	J5 (PS/2 connector), FPGA, J1, J2

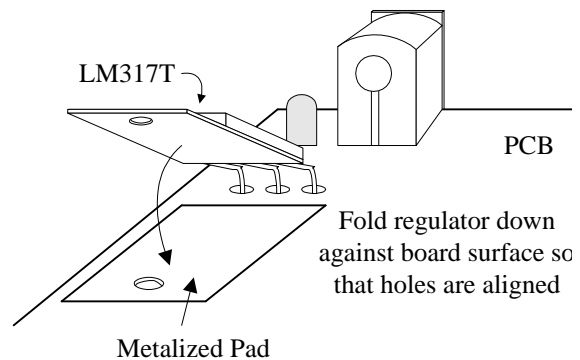
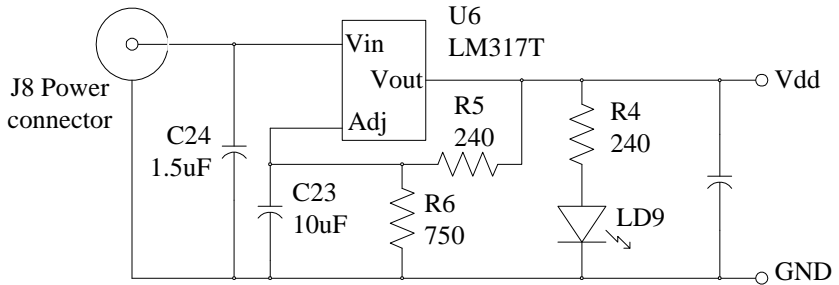
Circuit board

The FR-4 fiberglass circuit board uses a 1oz. copper, two layer, plated through-hole process with 6mil minimum trace size and .039" through-holes. Solder mask is provided on both sides, a silk-screen is provided on the component side, and all connectors can accommodate mechanical stays. Four 6/32"-sized corner holes are provided for stand-offs (to keep the board from contacting the work surface).

Power Supply

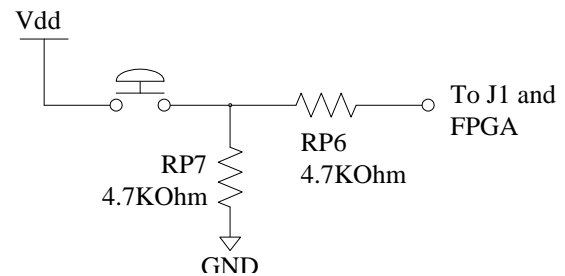
The circuits and components on the Digilab XL board require a 5VDC or 3.3VDC power supply. The board is equipped with a LM317T adjustable LDO voltage regulator (U6) that can produce either 5V or 3.3V depending on

the R6 resistor value (750 ohms for 5V; 390 ohms for 3.3V). The regulator will produce the selected voltage whenever a 6V-12VDC wall-plug transformer is attached at the power jack J8. Any 6-12VDC wall-plug transformer can be used, provided it has a coaxial 2.1mm center positive connector. The power circuit uses several bulk decoupling capacitors (C20, C23, C24) to produce a stable Vdd supply that typically has less than 50mV of ripple, even under heavy loads. An LED (LD9) in series with a 240-ohm resistor illuminates whenever power is present. With all IC's loaded in their sockets, including a 25MHz oscillator, the board consumes between 300 and 400 milliamps (depending on the size of FPGA-based circuits). Breadboard circuits or connected devices can markedly increase current consumption. For loads greater than about 500mA or power supply voltages greater than about 10V, the LM317T can be attached to the metalized pad on the circuit board with a 6/32 nut and screw to increase its heat-sinking capacity.



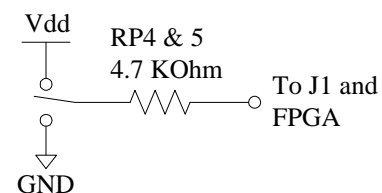
Push Buttons

Outputs from the four momentary-contact push buttons are normally low, and are driven high only while the button is actively pressed. The buttons nominally have a worst-case bounce time of about 1ms. The buttons drive the FPGA and J1 circuit nodes via a 4.7K resistor. The decoupling resistor is included so that the FPGA can use the button-connected pins as outputs if needed, without risking damage from the button state.



Slide switches

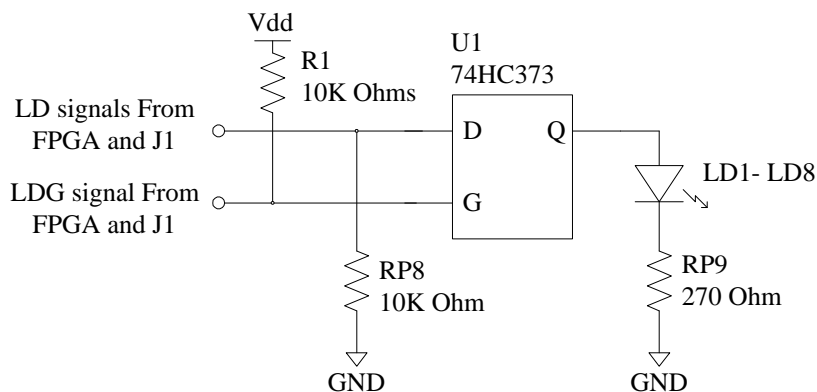
The eight slide switches can be used to connect either Vdd or GND to eight pins on the FPGA as well as to connections on J1. The switches exhibit about 2ms of bounce, and no active debouncing circuit is employed. As shown on the right, a 4.7K-ohm series resistor is used to provide nominal input protection, and to allow the switch-connected inputs to the FPGA to be used as outputs if necessary.



LEDs

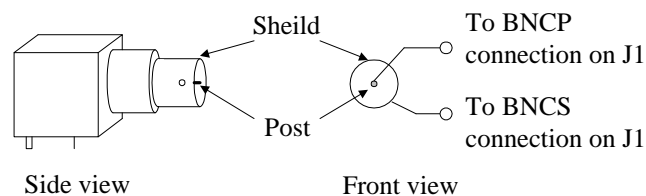
Eight red LEDs are provided for circuit outputs. The LED cathodes are tied to ground via 270-ohm resistors (in resistor pack RP9). The anodes are driven by U1, a 74HC373 CMOS D-register with 24mA per pin output current. Inputs to the 74HC373, each of which have a 10K pull-down resistor (RP8), arise from a common circuit node tied to both the FPGA and connections on J1. Thus, care should be taken not to drive the LED inputs from both the J1 connector and from the FPGA simultaneously.

A 74HC373 is used so that the LED drive signals can be decoupled from the FPGA, allowing the LED pins on the FPGA to serve a dual purpose if needed. The 74HC373 gate signal, which has a 10K pull-up (R1), can be driven from the FPGA or from a connection on J1.



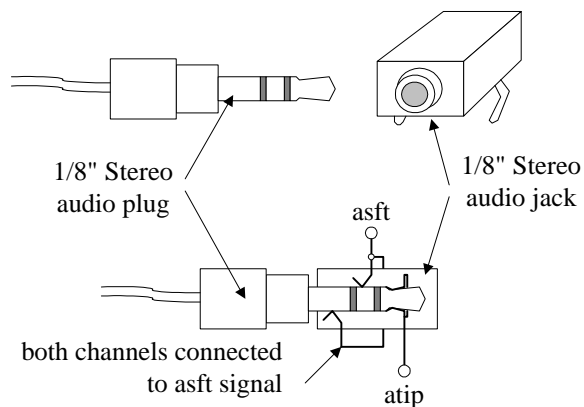
BNC connector

The BNC connector is provided to allow easy connection to test and measurement equipment. Both the shield and the center post are connected only to pins on the J1 connector to allow maximum flexibility. In a typical use, the BNC shield will be connected to GND using a jumper wire in the J1 connector, and the center post will be connected to the desired circuit node (again using a jumper wire).



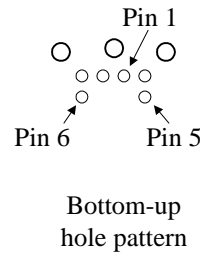
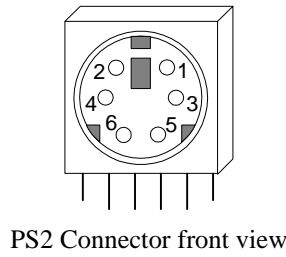
Audio connector

The two signals on the 1/8" audio connector are connected to pins on the J1 connector in order to allow easy connection of audio devices (e.g., speakers or microphones). Although the audio connector is a stereo connector, both channels have been tied into a common node. In typical use, the ASFT and ATIP signals will be connected to appropriate breadboard circuit nodes with jumper wire. To drive a speaker, these nodes can be tied to a dual-ended amplifier; to receive a microphone, they can be tied to a differential amplifier.



PS2 connector

The pin definitions for the PS2 connector are shown on the right. The clock and data signals (PS2C and PS2D) are connected to J2 (for easy connection of test and measurement equipment), and to the Xilinx FPGA. The PS2 signals are not routed to J1.

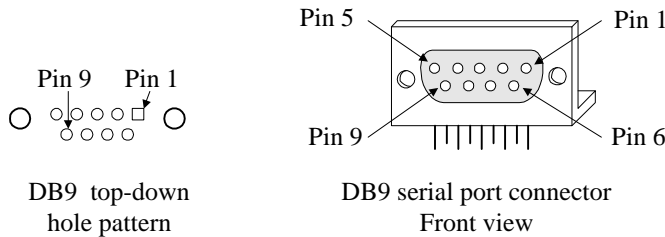


PS2 Pin Definitions

Pin	Function
1	Data
2	Reserved
3	GND
4	Vdd
5	Clock
6	Reserved

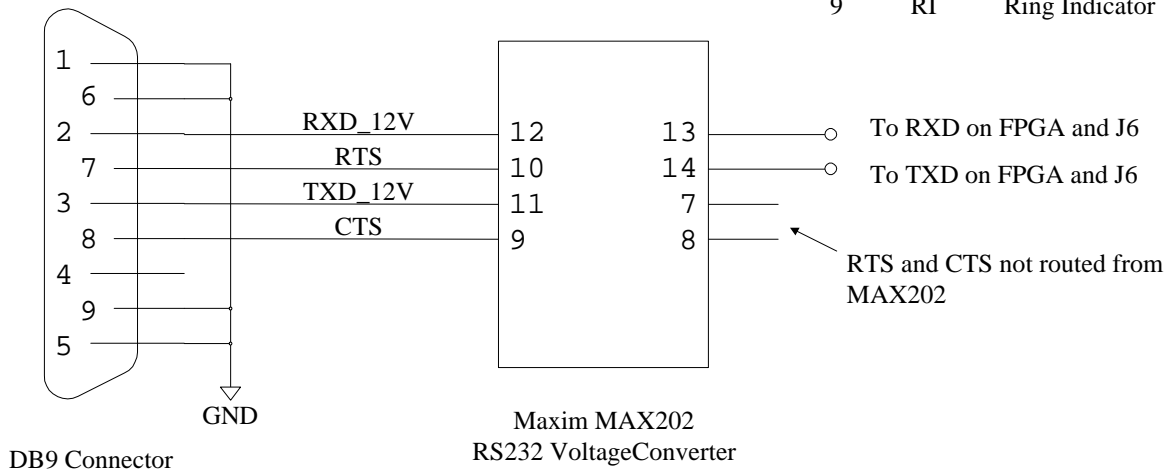
Serial Port

Serial port signal definitions and connector and circuit details are shown below. The Digilab serial port is compatible with RS232 two-wire communication protocols; that is, only the RXD and TXD signals from the serial port are routed to the FPGA. When using the serial port to communicate with a computer, a two-wire protocol such as XON/XOFF must be used. Specified RS232 voltages are +12V to +3V for a logic "0" and -12V to -3V for a logic "1" (the "dead area" between -3v and +3v is designed to absorb line noise). The Digilab board uses a MAX202 RS232 voltage converter to convert these signals to 5VDC for a logic "1" and GND for a logic "0".



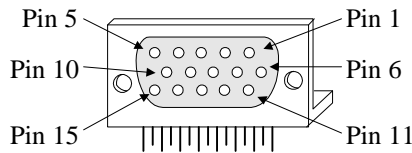
Serial Port Pin Definitions

Pin #	Name	Function
1	DTR	Data terminal ready
2	RXD	Received data
3	TXD	Transmitted data
4	DCD	Data carrier detect
5	SG	Signal ground
6	DSR	Data set ready
7	CTS	Clear to send
8	RTS	Request to send
9	RI	Ring Indicator

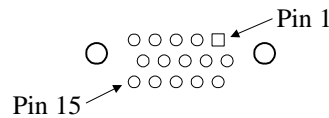


VGA connector

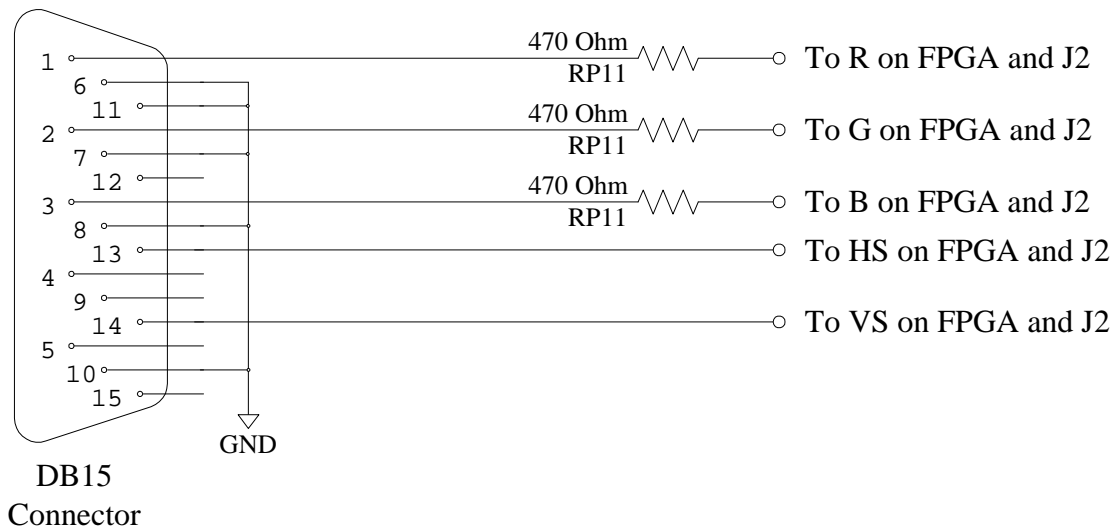
The five standard VGA signals (Red, Green, Blue, Horizontal Sync, and Vertical Sync) are routed from the FPGA to the VGA connector and to the J2 header (the J6 header allows for easy connection of test and measurement equipment). Standard VGA R, G, and B signals are terminated with a 75-ohm pull-down resistor. As shown below, a 470-ohm series resistor drives the R, G, and B signals, and the resistor-divider that is formed ensures the video signals never exceed the VGA-specified maximum of 0.7VDC. Note that each color is either on or off, which allows for eight different colors.



DB15 VGA connector
Front view



DB15 through-hole pattern as
seen from the top

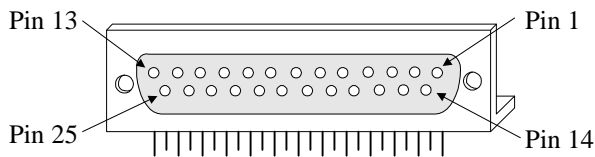


Parallel Port

All parallel port signals except pin 15 (SPP Error), pin 12 (SPP paper out), and pin 13 (SPP Select) are routed. Although the signal names reflect the Enhanced Parallel Port (EPP) mode, any protocol can be used for data transfer. Note that the full ECP protocol (including pin15) can be used if DB25 pin 15 is connected to one of the “open” signals on the FPGA (O1 – O5). All signals are also available at the J3 header for easy test and measurement equipment connection. All signals use 220 ohm series resistors to dampen possible line reflections and decouple the 5VDC port lines from the possible 3.3VDC Digilab Vdd voltage.

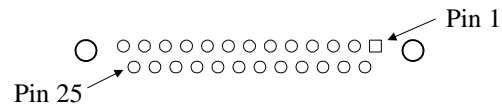
The Xilinx programming circuit, discussed in the following section, also uses the parallel port connector. Refer to that discussion for more information regarding the parallel port circuit.

Pin	EPP signal	EPP Function
1	Write Enable (O)	Low for read, High for write
2-9	Data bus (B)	Bidirectional data lines
10	Interrupt (I)	Interrupt/acknowledge input
11	Wait (I)	Bus handshake; low to ack
12	Spare	NOT CONNECTED
13	Spare	NOT CONNECTED
14	Data Strobe (O)	Low when data valid
15	Spare	NOT CONNECTED
16	Reset (O)	Low to reset
17	Address strobe (O)	Low when address valid
18-25	GND	System ground



DB25 parallel port connector

Front view

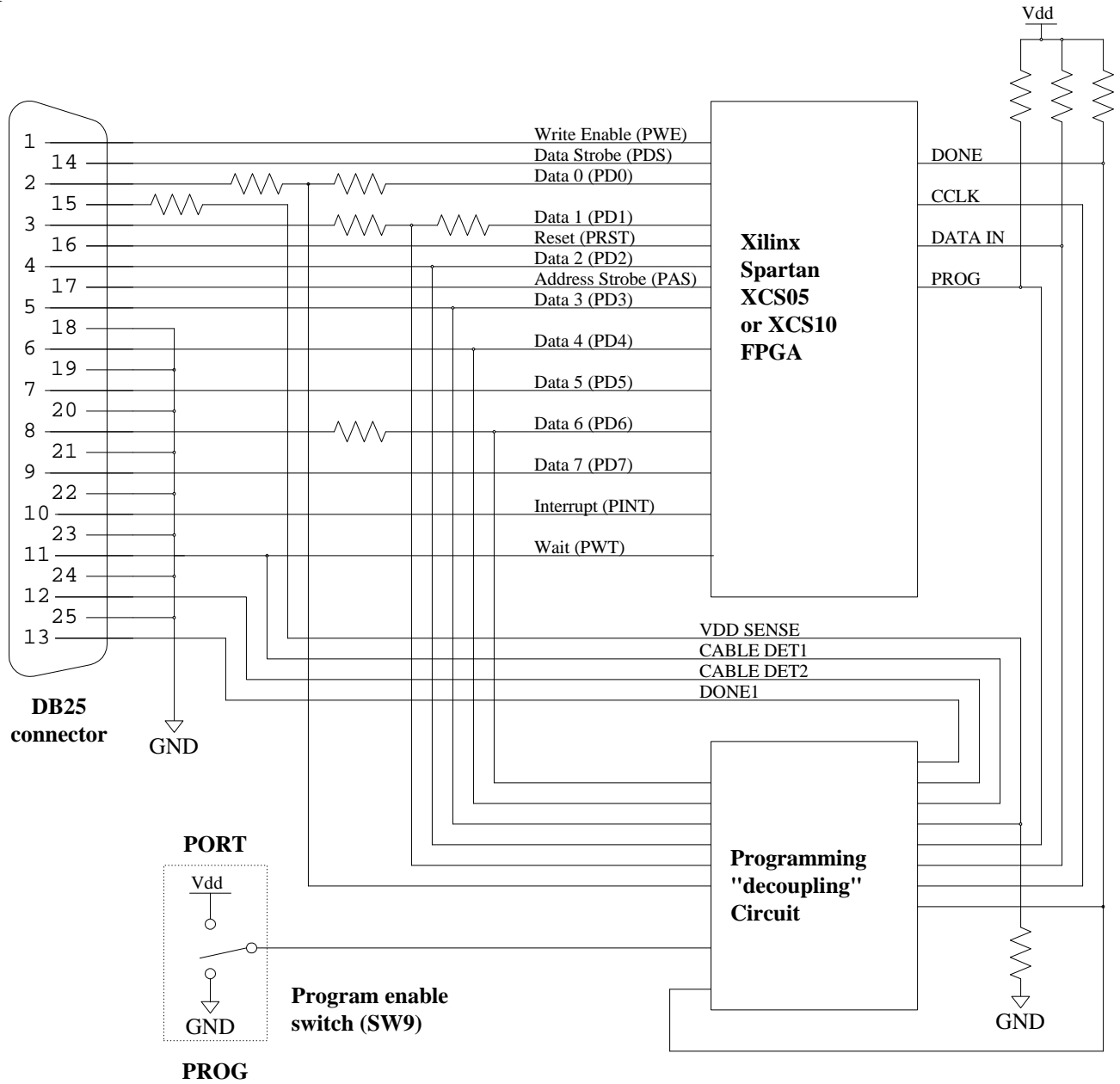


Xilinx Programming Circuit

The programming circuit (below) has been designed to accommodate a standard parallel cable and the Xilinx xchecker configuration protocol. The parallel cable will be auto-detected from within the Xilinx project manager, so that no external programming software is required. If the cable is not automatically detected the first time the Xilinx software is run with the board, it may be necessary to manually set the cable type in the Xilinx Design Manager “communications” pull-down menu.

The xchecker interface uses the DB25 connector and a standard parallel cable to connect to the FPGA programming port (readback functions are not supported). 4.7K pull-ups are provided on the PROG, INIT, and DONE signals. The parallel port interface serves both programming and functional needs. A circuit has been designed that allows the port to be manually switched from programming mode to port mode. Slide-switch SW9, located near the parallel port connector, can be placed in the “PROG” mode for programming and “PORT” mode to use the parallel port as a parallel port. Note that to program the FPGA and then use the parallel port, care must be taken in the application circuit design to not drive the port data signals until after the switch is moved to the “PORT” position. See the parallel port demo project at the Digilent website for more details.

The Digilab board can also accommodate a Xilinx SPROM in the 8-pin socket labeled ROM. To program from the ROM, load the ROM into the socket, place SW9 in the "PORT" position, and apply power to the board.



Clocks and Resets

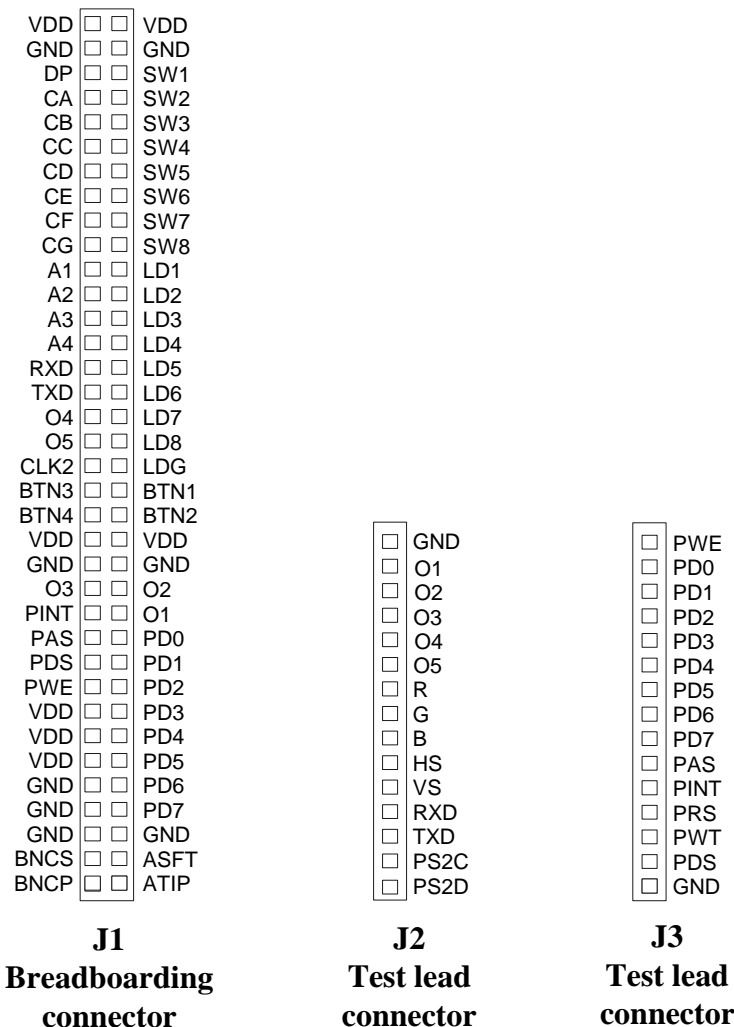
Two half-size (i.e., 8-pin DIP) sockets designated CLK1 and CLK2 have been provided near the FPGA for system clocks. Two clocks have been provided to accommodate peripherals that demand particular clocks (e.g., the VGA and serial devices), while still allowing a general system clock. CLK1, attached to the Spartan PGCK1 input, is considered the primary clock (pin 13), and CLK2 has been routed to the PGCK2 input (pin 35). No special system reset circuits have been provided – typically, one of the buttons is used as a functional system reset.

Data access connectors (J1, J2, J3)

J1 is a 72-pin socket connector that allows easy access to all Digilab signals for breadboarding purposes. All J1 pin definitions are provided in silk-screen labels immediately adjacent to the connector. In its intended use, individual wire-jumpers can be inserted into socket pins on J1 and into the breadboard area, thereby connecting breadboard circuit devices to the Digilab circuits. Note that J1 has seven pins providing GND connections and seven providing Vdd connections – these provide breadboard circuit with easy access to Vdd and GND.

J2 and J3 are single-row header connectors intended to allow easy connection of test and measurement equipment. Both J2 and J3 have GND pins that can serve as references for test and measurement equipment. All pins definitions are provided in silk-screen labels immediately adjacent to the connectors.

Schematic representations of the J1, J2, and J3 header connectors follow. Refer to the table of signal definitions provided earlier in this section.



FPGA

The Digilab board can accommodate a Xilinx Spartan XCS05, XCS10, XCS05XL, and XCS10XL FPGA in the 84-pin PLCC socket (the XL parts require a 390 ohm R6 for 3.3V operation). Any of these SRAM-based FPGA's may be programmed using a parallel cable or an SPROM (see above). The parallel cable provides an inexpensive programming solution that is compatible with the Xilinx CAD-tool cable detection software, so that the FPGA can be programmed without leaving the Xilinx environment. Refer to the Xilinx Spartan data sheet (<http://www.xilinx.com/partinfo/spartan.pdf>) for technical data regarding the FPGA's.

The table on the right shows all FPGA pin connections. In this pin-list, gray boxes indicate dedicated pins that are not available for use. Italicized names indicate dual-purpose pins; for these pins, the Xilinx function is shown first followed by Digilab's assignment in parenthesis.

Some FPGA signals, including the LED drive signals and the unassigned (or open) signals are available on the J1 prototyping connector. Care should be taken to ensure that these signals are not simultaneously driven by both the FPGA and by other drivers. If the FPGA is loaded in the U3 socket and external circuits must drive these signals, it would be best to tri-state the FPGA signals.

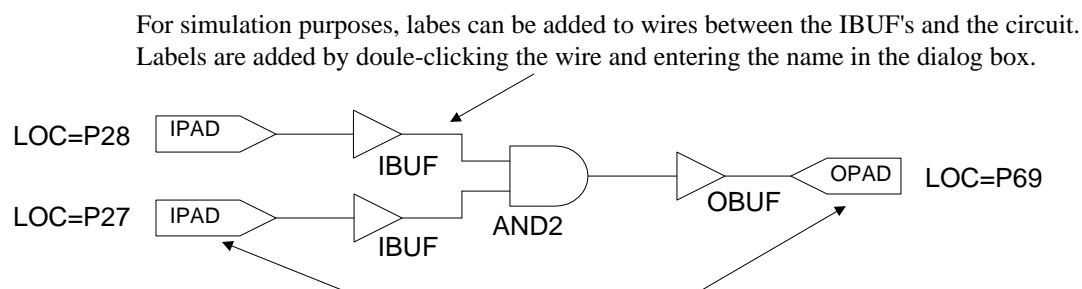
The parallel port connector can be used as the FPGA programming port or as a parallel port. When downloading a circuit that drives the parallel port data signals, ensure that the signals are not driven until SW9 has been moved to the PORT position. See the parallel port demo project on the Digilent web site.

Pin #	Function	Pin #	Function	Pin #	Function
1	GND	29	O1	57	BTN3
2	Vdd	30	M1_NC	58	BTN2
3	PWE	31	GND	59	BTN1
4	PD0	32	MODE	60	LD8
5	PD1	33	Vdd	61	LD7
6	PD2	34	M2_NC	62	LD6
7	PD3	35	CLK2	63	Vdd
8	PD4	36	O2	64	GND
9	PAS	37	O3	65	LD5
10	PRS	38	A4	66	LD4
11	Vdd	39	A3	67	LD3
12	GND	40	A2	68	LD2
13	CLK1	41	INIT (O4)	69	LD1
14	PDS	42	Vdd	70	LDG
15	PWT	43	GND	71	DIN (O5)
16	PD5	44	A1	72	DOUT (RXD)
17	PD7	45	CG	73	CCLK
18	PD6	46	CF	74	Vdd
19	SW8	47	CE	75	TXD (PINT)
20	SW7	48	CD	76	GND
21	GND	49	CC	77	R
22	Vdd	50	CB	78	G
23	SW6	51	CA	79	B
24	SW5	52	GND	80	HS
25	SW4	53	DONE	81	VS
26	SW3	54	Vdd	82	PS2C
27	SW2	55	PROG	83	PS2D
28	SW1	56	BTN4	84	PINT

Any CAD-tool-designed circuit that requires fewer than about 5K – 10K gates can be programmed into the Xilinx FPGA. However, the circuit description must first be transformed into the format required by the FPGA. This transformation proceeds in several steps, typically beginning with an EDIF, VHDL, or Verilog file format and ending with a Xilinx “bit” file format. Xilinx (of course) produces a tool that accomplishes this transformation, which is available in the Xilinx Alliance and Foundation products (see the Xilinx web site). Although other methods of transforming files may be available, only the Xilinx solution has been used with the Digilab board. Although the use of the Xilinx tools is beyond the scope of this document, Xilinx has several good tutorials and helpful documentation available at their web site.

All signals on the Digilab board that connect the buttons, switches, and LEDs to the J1 connector are connected to the Xilinx FPGA chip as well. Any circuit implemented in the FPGA can use the buttons and switches as inputs and the LEDs as outputs. When the Digilab board was fabricated, the buttons, switches, and LEDs were connected to particular pins on the FPGA (see the table in the previous section for all FPGA pin definitions). To connect an FPGA-based circuit to these devices, you must include information in your schematic to “map” circuit inputs and outputs to particular FPGA pins. Mapping is accomplished by including special components in your schematic called IPADs, IBUFs, OPADs and OBUFs. These components exist solely to allow you to define physical pin connections, and so they only need be used in circuit schematics that you intend to download.

Once you have a complete and error-free schematic, you may add IBUFs and IPADs to all inputs, and OBUFs and OPADs to all outputs. Then, the IPADs and OPADs can be connected to particular pins by double-clicking the pads and entering the “LOC” parameter and pin number in the appropriate fields (Name and Description, respectively). In the example circuit below, two switches (SW1 on pin P28 and SW2 on pin P27) are connected via an AND gate to LED1 (LD1 on pin P69). If this circuit were downloaded to the FPGA, then LD1 would illuminate whenever SW1 and SW2 were asserted.



"LOC" parameters are added by double-clicking the pad symbol and entering **LOC** in the Parameters Name field and **Pnn** in the Parameters Description field, and then pressing **Add** and **OK**.

Once all IPADs, IBUFs, OPADs, and OBUFs have been added and edited with pin locations, you can begin the implementation process by choosing the “Implementation” button from the Xilinx main screen. In the first dialog box that appears, choose Yes to update the netlist from the schematic editor. In the second dialog box, make sure the device is S10PC84 and speed is 3 before proceeding; the version and revision names can use the defaults. Press the Run button, and then wait for the status window showing Translate, Map, Place & Route, Timing, and Configure processes to terminate. Before proceeding, make sure that the Digilab board is powered on and connected to the PC via the parallel cable, and that SW9 is in the PROG position. Then select the Programming option from the Xilinx main window, and “hardware debugger” from the subsequent dialog box. The cable should be auto-detected; if not, manually choose the parallel cable in the Cable → communications dialog box.

Once the cable has been detected, you can download your design simply by double-clicking on the appropriate file name in the hardware debugger window.

Two 8-pin DIP clock sockets have been provided for use with the FPGA. Labeled CLK1 and CLK2, they connect to pin 13 (Xilinx primary clock buffer #1) and pin 35 (Xilinx primary clock buffer #2). Clock sources up to 80MHz have been successfully used with the board.

The FPGA programming circuit has been designed to accommodate a standard parallel cable or an SPROM. When programming the FPGA from within the Xilinx CAD tool, the parallel cable will be automatically detected (so no external programming software is required). If a cable is not automatically detected the first time the Xilinx software is run with the board, it may be necessary to manually set the cable type in the Xilinx Design Manager “communications” pull-down menu.

The parallel port interface serves both programming and functional needs. A circuit has been designed that allows the port to be manually switched from programming mode to port mode. Slide-switch SW9, located near the parallel port connector, must be placed in the “PROG” mode for programming from a host PC and “PORT” mode to use the parallel port as a parallel port or to program from an onboard ROM at power-up. Note that to program the FPGA and then use the parallel port, care must be taken in the application circuit design to not drive the port data signals until after the switch is moved to the “PORT” position.