October 1997

National Semiconductor

# LM75
# Digital Temperature Sensor and Thermal Watchdog with Two-Wire Interface

## General Description

The LM75 is a temperature sensor, Delta-Sigma analog-to-digital converter, and digital over-temperature detector with I²C® interface. The host can query the LM75 at any time to read temperature. The open-drain Overtemperature Shutdown (O.S.) output becomes active when the temperature exceeds a programmable limit. This pin can operate in either "Comparator" or "Interrupt"mode.

The host can program both the temperature alarm threshold ($T_{OS}$) and the temperature at which the alarm condition goes away ($T_{HYST}$). In addition, the host can read back the contents of the LM75's $T_{OS}$ and $T_{HYST}$ registers. Three pins (A0, A1, A2) are available for address selection. The sensor powers up in Comparator mode with default thresholds of 80˚C $T_{OS}$ and 75˚C $T_{HYST}$.

The LM75's 3.0V to 5.5V supply voltage range, low supply current and I²C interface make it ideal for a wide range of applications. These include thermal management and protection applications in personal computers, electronic test equipment, and office electronics.

## Features

- SOP-8 and Mini SOP-8 (MSOP) packages save space
- I²C Bus interface
- Separate open-drain output pin operates as interrupt or comparator/thermostat output
- Register readback capability
- Power up defaults permit stand-alone operation as thermostat
- Shutdown mode to minimize power consumption
- Up to 8 LM75s can be connected to a single bus

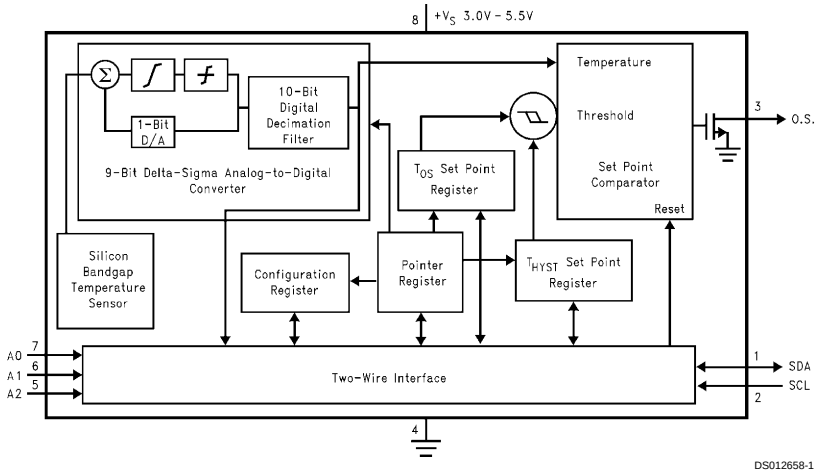
## Key Specifications

| | | |
|---|---|---|
| ■ Supply Voltage | | 3.0V to 5.5V |
| ■ Supply Current | operating | 250 µA (typ) |
| | | 1 mA (max) |
| | shutdown | 1 µA (typ) |
| ■ Temperature Accuracy | −25˚C to 100˚C | ±2˚C(max) |
| | −55˚C to 125˚C | ±3˚C(max) |

## Applications

- System Thermal Management
- Personal Computers
- Office Electronics
- Electronic Test Equipment

## Simplified Block Diagram

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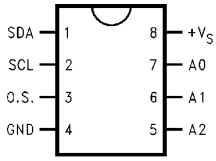
I²C® is a registered trademark of Philips Corporation.

## Connection Diagram

**SOP-8 and Mini SOP-8**




DS012658-2

## Ordering Information

| Order Number | NS Package Number | Supply Voltage | Transport Media |
|---|---|---|---|
| LM75CIM-3 | M08A (SOP-8) | 3.3V | |
| LM75CIMX-3 | M08A (SOP-8) | 3.3V | 2500 Units on Tape and Reel |
| LM75CIMM-3 | MUA08A (MSOP-8) | 3.3V | 250 Units in Rail |
| LM75CIMMX-3 | MUA08A (MSOP-8) | 3.3V | 3500 Units on Tape and Reel |
| LM75CIM-5 | M08A (SOP-8) | 5V | |
| LM75CIMX-5 | M08A (SOP-8) | 5V | 2500 Units on Tape and Reel |
| LM75CIMM-5 | MUA08A (MSOP-8) | 5V | 250 Units in Rail |
| LM75CIMMX-5 | MUA08A (MSOP-8) | 5V | 3500 Units on Tape and Reel |

## Pin Description

| Label | Pin # | Function | Typical Connection |
|---|---|---|---|
| SDA | 1 | $I^2C$ Serial Bi-Directional Data Line | From Controller |
| SCL | 2 | $I^2C$ Clock Input | From Controller |
| O.S. | 3 | Overtemperature Shutdown Open Collector Output | Pull Up Resistor, Controller Interrupt Line |
| GND | 4 | Power Supply Ground | Ground |
| $+V_S$ | 8 | Positive Supply Voltage Input | DC Voltage from 3V to 5.5V |
| A0–A2 | 7,6,5 | User-Set $I^2C$ Address Inputs | Ground (Low, “0”) or $+V_S$ (High, “1”) |

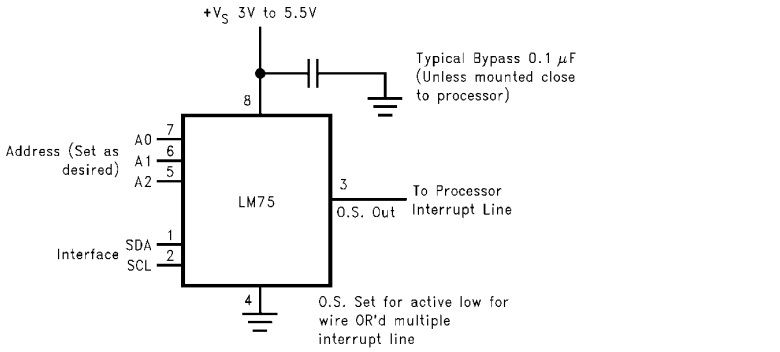



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**FIGURE 1. Typical Application**

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage | −0.3V to 6.5V |
| Voltage at any Pin | −0.3V to +$V_S$ + 0.3V |
| Input Current at any Pin (Note 2) | 5 mA |
| Package Input Current (Note 2) | 20 mA |
| O.S. Output Sink Current | 10 mA |
| O.S. Output Voltage | 6.5V |
| Storage Temperature | −65˚C to +150˚C |
| Soldering Information, Lead Temperature | |
| SOP and MSOP Package (Note 3) | |
| Vapor Phase (60 seconds) | 215˚C |
| Infrared (15 seconds) | 220˚C |
| ESD Susceptibility (Note 4) | |
| Human Body Model | 950V |
| Machine Model | 200V |

## Operating Ratings

| | |
|---|---|
| Specified Temperature Range | $T_{MIN}$ to $T_{MAX}$ |
| (Note 5) | −55˚C to +125˚C |
| Supply Voltage Range (+$V_S$) | +3.0V to +5.5V |

## Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for +$V_S$=+5 Vdc for LM75CIM-5 and LM75CIMM-5 and +$V_S$=+3.3 Vdc for LM75CIM-3 and LM75CIMM-3 (Note 6). **Boldface limits apply for $T_A$ = $T_J$ = $T_{MIN}$ to $T_{MAX}$;** all other limits $T_A$= $T_J$=+25˚C, unless otherwise noted.

| Parameter | Conditions | Typical (Note 12) | Limits (Note 7) | Units (Limit) |
|---|---|---|---|---|
| Accuracy | $T_A$ = −25˚C to +100˚C | | **±2.0** | ˚C (max) |
| | $T_A$ = −55˚C to +125˚C | | **±3.0** | |
| Resolution | | 9 | | Bits |
| Temperature Conversion Time | (Note 8) | 100 | | ms |
| Quiescent Current | $I^2C$ Inactive | 0.25 | | mA |
| | $I^2C$ Active | | **1.0** | mA (max) |
| | Shutdown Mode | 1 | | µA |
| O.S. Output Saturation Voltage | $I_{OUT}$ = 4.0 mA | | **0.8** | V (max) |
| | (Note 9) | | | |
| O.S. Delay | (Note 10) | | **1** | Conversions (min) |
| | | | **6** | Conversions (max) |
| $T_{OS}$ Default Temperature | (Note 11) | 80 | | ˚C |
| $T_{HYST}$ Default Temperature | (Note 11) | 75 | | ˚C |

## Logic Electrical Characteristics

**DIGITAL DC CHARACTERISTICS**

Unless otherwise noted, these specifications apply for +$V_S$=+5 Vdc for LM75CIM-5 and LM75CIMM-5 and +$V_S$=+3.3 Vdc for LM75CIM-3 and LM75CIMM-3 . **Boldface limits apply for $T_A$ = $T_J$ = $T_{MIN}$ to $T_{MAX}$;** all other limits $T_A$= $T_J$=+25˚C, unless otherwise noted.

| Symbol | Parameter | Conditions | Typical (Note 12) | Limits (Note 7) | Units (Limit) |
|---|---|---|---|---|---|
| $V_{IN(1)}$ | Logical “1” Input Voltage | | | **+$V_S$ x 0.7** | V (min) |
| | | | | **+$V_S$+0.5** | V (max) |
| $V_{IN(0)}$ | Logical “0” Input Voltage | | | **−0.3** | V (min) |
| | | | | **+$V_S$ x 0.3** | V (max) |
| $I_{IN(1)}$ | Logical “1” Input Current | $V_{IN}$ = 5V | 0.005 | **1.0** | µA (max) |
| $I_{IN(0)}$ | Logical “0” Input Current | $V_{IN}$ = 0V | −0.005 | **−1.0** | µA (max) |
| $C_{IN}$ | All Digital Inputs | | 20 | | pF |
| $I_{OH}$ | High Level Output Current | $V_{OH}$ = 5V | | **100** | µA (max) |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = 3 mA | | **0.4** | V (max) |
| $t_{OF}$ | Output Fall Time | $C_L$ = 400 pF | | **250** | ns (max) |
| | | $I_O$ = 3 mA | | | |

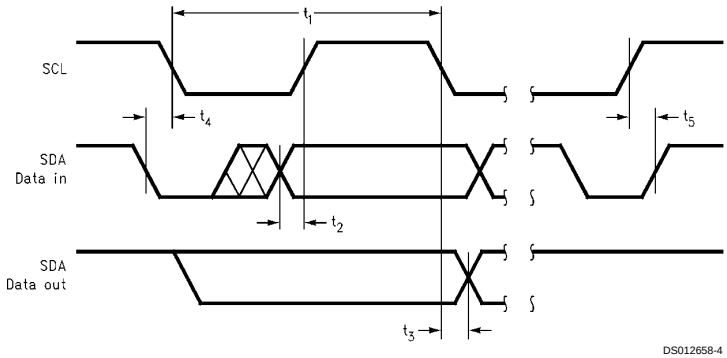
## Logic Electrical Characteristics (Continued)

**I²C DIGITAL SWITCHING CHARACTERISTICS**

Unless otherwise noted, these specifications apply for+$V_S$=+5 Vdc for LM75CIM-5 and LM75CIMM-5 and +$V_S$=+3.3 Vdc for LM75CIM-3 and LM75CIMM-3 , $C_L$ (load capacitance) on output lines = 80 pF unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J$ = +25˚C, unless otherwise noted.

The switching characteristics of the LM75 fully meet or exceed the published specifications of the I²C bus. The following parameters are the timing relationships between SCL and SDA signals related to the LM75. They are not the I²C bus specifications.

| Symbol | Parameter | Conditions | Typical (Note 12) | Limits (Note 7) | Units (Limit) |
|---|---|---|---|---|---|
| $t_1$ | SCL (Clock) Period | | | **2.5** | µs(min) |
| $t_2$ | Data in Set-Up Time to SCL High | | | **100** | ns(min) |
| $t_3$ | Data Out Stable after SCL Low | | | **0** | ns(min) |
| $t_4$ | SDA Low Set-Up Time to SCL Low (Start Condition) | | | **100** | ns(min) |
| $t_5$ | SDA High Hold Time after SCL High (Stop Condition) | | | **100** | ns(min) |




**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

**Note 2:** When the input voltage ($V_I$) at any pin exceeds the power supplies ($V_I$ < GND or $V_I$ > +$V_S$) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceedthe power supplies with an input current of 5 mA to four.

**Note 3:** See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

**Note 4:** Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin.

**Note 5:** LM75 $\theta_{JA}$ (thermal resistance , junction-to-ambient) when attached to a printed circuit board with 2 oz. foil similar to the one shown in *Figure 3*is summarized in the table below:.

| Device Number | NS Package Number | Thermal Resistance ($\theta_{JA}$) |
|---|---|---|
| LM75CIM-3, LM75CIM-5 | M08A | 200˚C/W |
| LM75CIMM-3, LM75CIMM-5 | MUA08A | 250˚C/W |

**Note 6:** Both part numbers of the LM75 will operate properly over the +$V_S$ supply voltage range of 3V to 5.5V. The devices are tested and specified for rated accuracy at their nominal supply voltage. Accuracy will typically degrade 1˚C/V of variation in +$V_S$ as it varies from the nominal value.

**Note 7:** Limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

**Note 8:** This specification is provided only to indicate how often temperature data is updated. The LM75 can be read at any time without regard to conversion state (and will yield last conversion result). If a conversion is in process it will be interrupted and restarted after the end of the read.

**Note 9:** For best accuracy, minimize output loading. Higher sink currents can affect sensor accuracy with internal heating. This can cause an error of 0.64˚C at full rated sink current and saturation voltage based on junction-to-ambient thermal resistance.

**Note 10:** O.S. Delay is user programmable up to 6 “over limit” conversions before O.S. is set to minimize false tripping in noisy environments.

**Note 11:** Default values set at power up.

**Note 12:** Typicals are at $T_A$ = 25˚C and represent most likely parametric norm.

## Logic Electrical Characteristics (Continued)

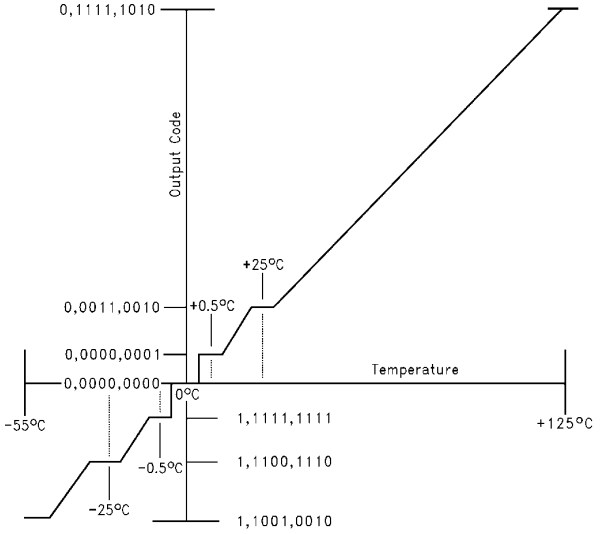



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**FIGURE 2. Temperature-to-Digital Transfer Function (Non-linear scale for clarity)**

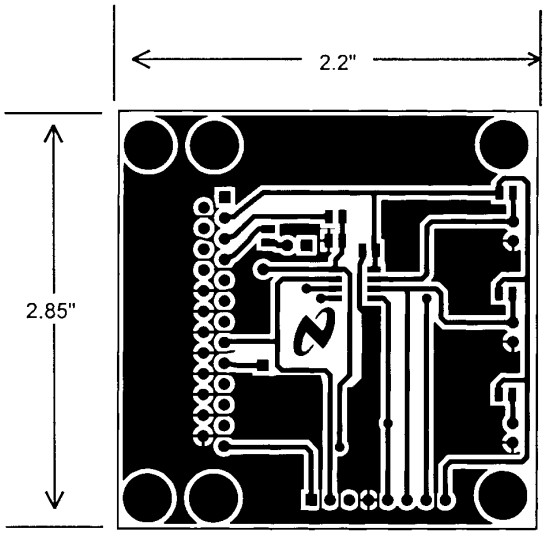


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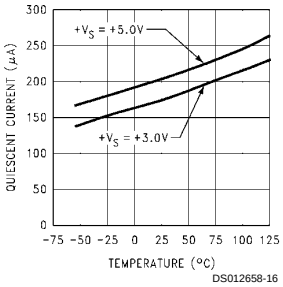
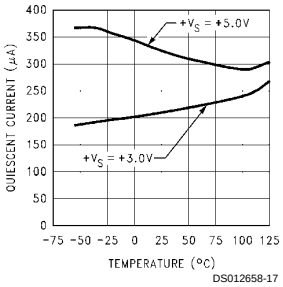
**FIGURE 3. Printed Circuit Board Used for Thermal Resistance Specifications**

## Typical Performance Characteristics

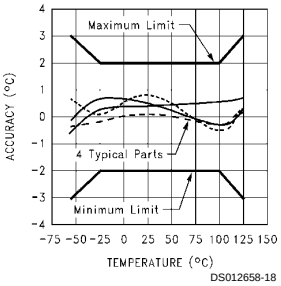
**Static Quiescent Current vs Temperature**




**Dynamic Quiescent Current vs Temperature**




**Accuracy vs Temperature**




## 1.0 Functional Description

The LM75 temperature sensor incorporates a band-gap type temperature sensor and 9-bit ADC (Delta-Sigma Analog-to-Digital Converter). The temperature data output of the LM75 is available at all times via the $I^2C$ bus. If a conversion is in progress, it will be stopped and restarted after the read. A digital comparator is also incorporated that compares a series of readings, the number of which is user-selectable, to user-programmable setpoint and hysteresis values. The comparator trips the O.S. output line, which is programmable for mode and polarity.

### 1.1 O.S. OUTPUT, $T_{OS}$ AND $T_{HYST}$ LIMITS

In Comparator mode the O.S. Output behaves like a thermostat. The output becomes active when temperature exceeds the $T_{OS}$ limit, and leaves the active state when the temperature drops below the $T_{HYST}$ limit. In this mode the O.S. output can be used to turn a cooling fan on, initiate an emergency system shutdown, or reduce system clock speed. Shutdown mode does not reset O.S. state in a comparator mode.

In Interrupt mode exceeding $T_{OS}$ also makes O.S. active but O.S. will remain active indefinitely until reset by reading any register via the $I^2C$ interface. Once O.S. has been activated by crossing $T_{OS}$, then reset, it can be activated again only by Temperature going below $T_{HYST}$. Again, it will remain active indefinitely until being reset by a read. Placing the LM75 in shutdown mode also resets the O.S. Output.

### 1.2 DEFAULT MODES

LM75 always powers up in a known state. LM75 power up default conditions are:

1. Comparator mode
2. $T_{OS}$ set to 80˚C
3. $T_{HYST}$ set to 75˚C
4. O.S. active low
5. Pointer set to “00”; Temperature Register

With these operating conditions LM75 can act as a stand-alone thermostat with the above temperature settings. Connection to an $I^2C$ bus is not required.

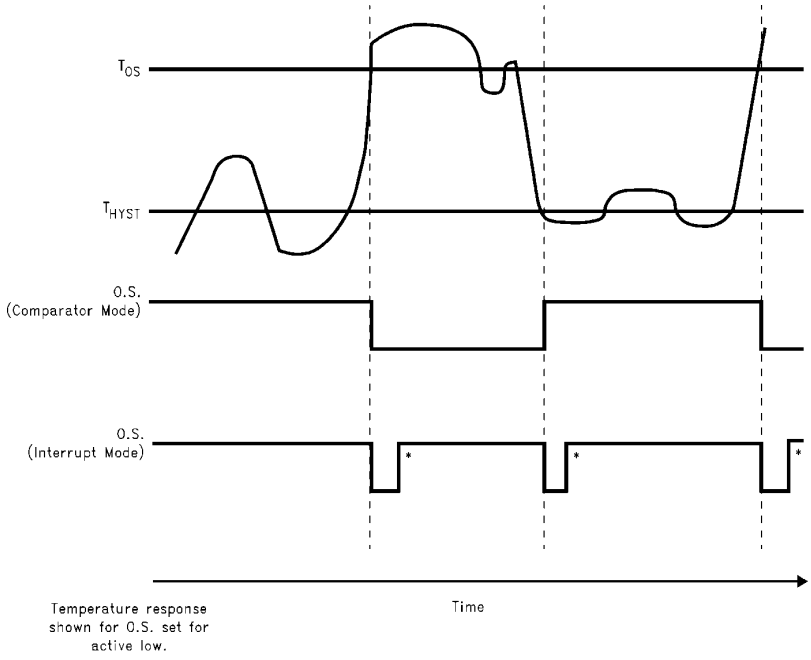
### 1.3 $I^2C$ BUS INTERFACE

The LM75 operates as a slave on the $I^2C$ bus, so the SCL line is an input (no clock is generated by the LM75) and the SDA line is a bi-directional serial data path. According to $I^2C$ bus specifications, the LM75 has a 7-bit slave address. The four most significant bits of the slave address are hard wired inside the LM75 and are “1001”. The three least significant bits of the address are assigned to pins A2–A0, and are set by connecting these pins to ground for a low, (0); or to $+V_S$ for a high, (1).

Therefore, the complete slave address is:

| 1 | 0 | 0 | 1 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|
| MSB | | | | | | LSB |

## 1.0 Functional Description (Continued)

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**Note 13:** These interrupt mode resets of O.S. occur only when LM75 is read or placed in shutdown. Otherwise, O.S. would remain active indefinitely for any event.

**FIGURE 4. O.S. Output Temperature Response Diagram**

## 1.0 Functional Description (Continued)

### 1.4 TEMPERATURE DATA FORMAT

Temperature data can be read from the Temperature, $T_{OS}$ Set Point, and $T_{HYST}$ Set Point registers; and written to the $T_{OS}$ Set Point, and $T_{HYST}$ Set Point registers. Temperature data is represented by a 9-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.5˚C:

| Temperature | Digital Output | |
|---|---|---|
| | Binary | Hex |
| +125˚C | 0 1111 1010 | 0FAh |
| +25˚C | 0 0011 0010 | 032h |
| +0.5˚C | 0 0000 0001 | 001h |
| 0˚C | 0 0000 0000 | 000h |
| −0.5˚C | 1 1111 1111 | 1FFh |
| −25˚C | 1 1100 1110 | 1CEh |
| −55˚C | 1 1001 0010 | 192h |

### 1.5 SHUTDOWN MODE

Shutdown mode is enabled by setting the shutdown bit in the Configuration register via the $I^2C$ bus. Shutdown mode reduces power supply current to 1 µA typical. In Interrupt mode O.S. is reset if previously set and is undefined in Comparator mode during shutdown. The $I^2C$ interface remains active. Activity on the clock and data lines of the $I^2C$ bus may slightly increase shutdown mode quiescent current. $T_{OS}$, $T_{HYST}$, and Configuration registers can be read from and written to in shutdown mode.

### 1.6 FAULT QUEUE

A fault queue of up to 6 faults is provided to prevent false tripping of O.S. when the LM75 is used in noisy environments. The number of faults set in the queue must occur consecutively to set the O.S. output.

### 1.7 COMPARATOR/INTERRUPT MODE

As indicated in the O.S. Output Temperature Response Diagram, *Figure 4*, the events that trigger O.S. are identical for either Comparator or Interrupt mode. The most important difference is that in Interrupt mode the O.S. will remain set indefinitely once it has been set. To reset O.S. while in Interrupt mode, perform a read from any register in the LM75.

### 1.8 O.S. OUTPUT

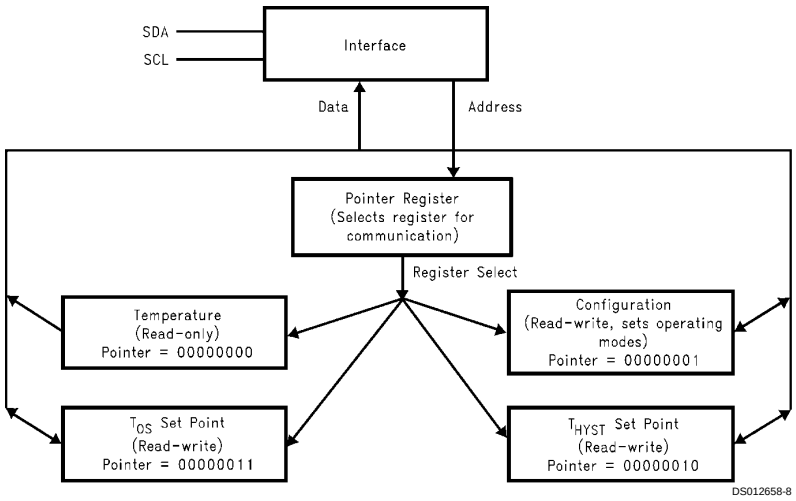
The O.S. output is an open-drain output and does not have an internal pull-up. A "high" level will not be observed on this pin until pull-up current is provided from some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible. This will minimize any errors due to internal heating of the LM75. The maximum resistance of the pull up, based on LM75 specification for High Level Output Current, to provide a 2V high level, is 30 kΩ.

### 1.9 O.S. POLARITY

The O.S. output can be programmed via the configuration register to be either active low (default mode), or active high. In active low mode the O.S. output goes low when triggered exactly as shown on the O.S. Output Temperature Response Diagram, *Figure 4*. Active high simply inverts the polarity of the O.S. output.

## 1.0 Functional Description (Continued)

### 1.10 INTERNAL REGISTER STRUCTURE




There are four data registers in the LM75, selected by the Pointer register. At power-up the Pointer is set to "00"; the location for the Temperature Register. The Pointer register latches whatever the last location it was set to. In Interrupt Mode, a read from the LM75, or placing the device in shutdown mode, resets the O.S. output. All registers are read and write, except the Temperature register which is read only.

A write to the LM75 will always include the address byte and the Pointer byte. A write to the Configuration register requires one data byte, and the $T_{OS}$ and $T_{HYST}$ registers require two data bytes.

Reading the LM75 can take place either of two ways: If the location latched in the Pointer is correct (most of the time it is expected that the Pointer will point to the Temperature register because it will be the data most frequently read from the LM75), then the read can simply consist of an address byte, followed by retrieving the corresponding number of data bytes. If the Pointer needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a read.

The first data byte is the most significant byte with most significant bit first, permitting only as much data as necessary to be read to determine temperature condition. For instance, if the first four bits of the temperature data indicates an overtemperature condition, the host processor could immediately take action to remedy the excessive temperatures. At the end of a read, the LM75 can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the LM75 to stop in a state where the SDA line is held low as shown in *Figure 5*. This can prevent any further bus communication until at least 9 additional clock cycles have occurred. Alternatively, the master can issue clock cycles until SDA goes high, at which time issuing a "Stop" condition will reset the LM75.

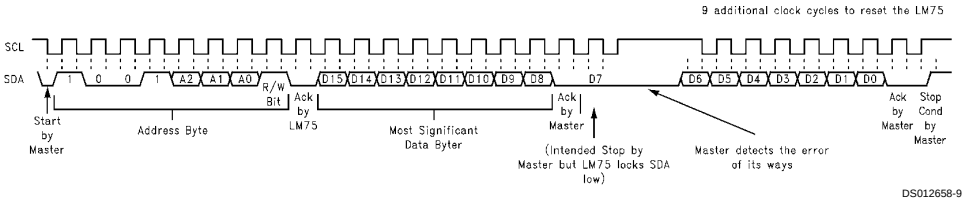



**FIGURE 5. Inadvertent 8-Bit Read from 16-Bit Register where D7 is Zero ("0")**

## 1.0 Functional Description (Continued)

### 1.11 POINTER REGISTER

(Selects which registers will be read from or written to):

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Register Select | |

P0-P1: Register Select:

| P1 | P0 | Register |
|---|---|---|
| 0 | 0 | Temperature (Read only) (Power-up default) |
| 0 | 1 | Configuration (Read/Write) |
| 1 | 0 | $T_{HYST}$ (Read/Write) |
| 1 | 1 | $T_{OS}$ (Read/Write) |

P2–P7: Must be kept zero.

### 1.12 TEMPERATURE REGISTER

(Read Only):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | LSB | X | X | X | X | X | X | X |

D0–D6: Undefined

D7–D15: Temperature Data. One LSB = 0.5˚C. Two's complement format.

### 1.13 CONFIGURATION REGISTER

(Read/Write):

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Fault Queue | | O.S. Polarity | Cmp/Int | Shutdown |

Power up default is with all bits "0" (zero).

D0: Shutdown: When set to 1 the LM75 goes to low power shutdown mode.

D1: Comparator/Interrupt mode: 0 is Comparator mode, 1 is Interrupt mode.

D2: O.S. Polarity: 0 is active low, 1 is active high. O.S. is an open-drain output under all conditions.

D3–D4: Fault Queue: Number of faults necessary to detect before setting O.S. output to avoid false tripping due to noise:

| D4 | D3 | Number of Faults |
|---|---|---|
| 0 | 0 | 1 (Power-up default) |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

D5–D7: These bits are used for production testing and must be kept zero for normal operation.

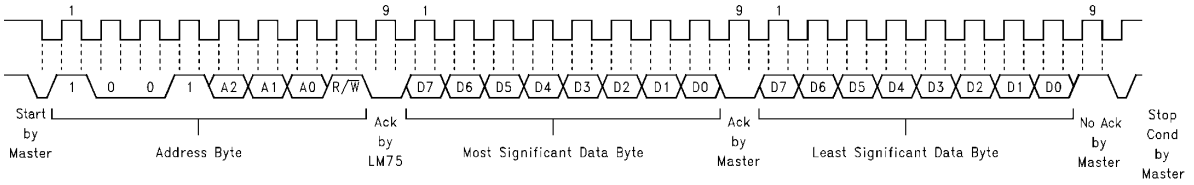
### 1.14 $T_{HYST}$ AND $T_{OS}$ REGISTER

(Read/Write):

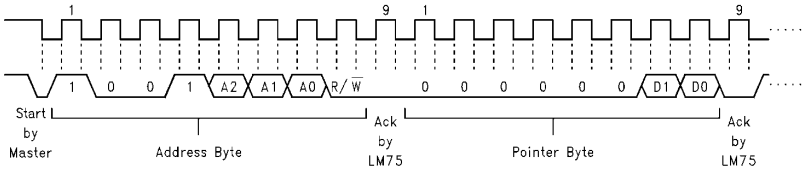
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | LSB | X | X | X | X | X | X | X |

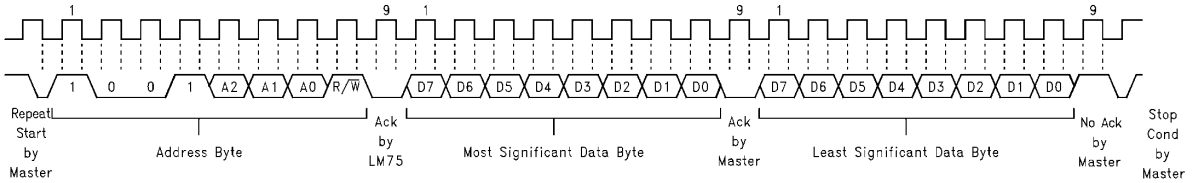
D0–D6: Undefined

D7–D15: $T_{HYST}$ Or $T_{OS}$ Trip Temperature Data. Power up default is $T_{OS}$ = 80˚C, $T_{HYST}$ = 75˚C.

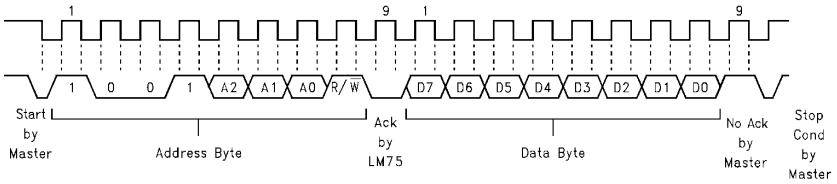



(a) Typical 2−Byte Read From Preset Pointer Location Such as Temp, $T_{OS}$, $T_{HYST}$




(b) Typical Pointer Set Followed by Immediate Read for 2−Byte Register such as Temp, $T_{OS}$, $T_{HYST}$

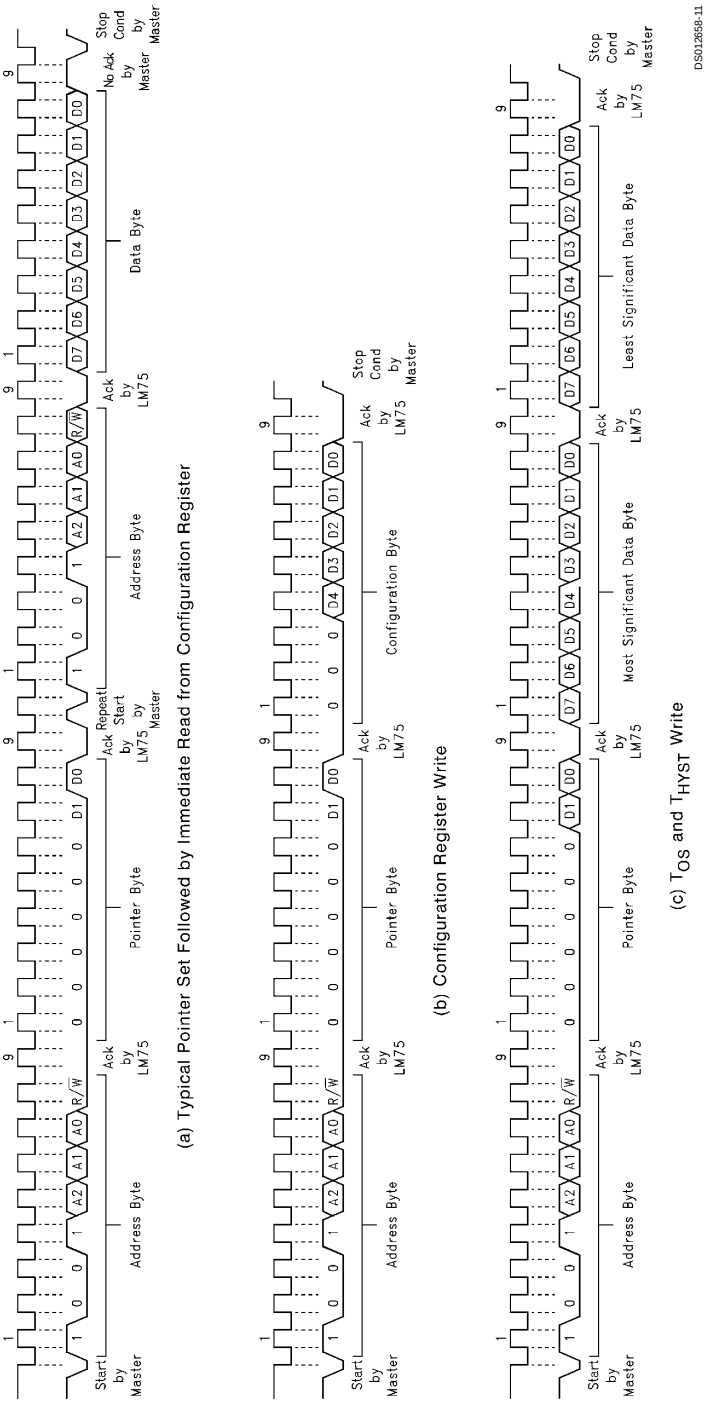



(c) Typical 1−Byte Read From Configuration Register With Preset Pointer

DS012658-10

**FIGURE 6. Timing Diagram**

## 2.0 I²C Timing Diagrams (Continued)




(a) Typical Pointer Set Followed by Immediate Read from Configuration Register

(b) Configuration Register Write

(c) $T_{OS}$ and $T_{HYST}$ Write

**FIGURE 7. Timing Diagrams (Continued)**

## 3.0 Application Hints

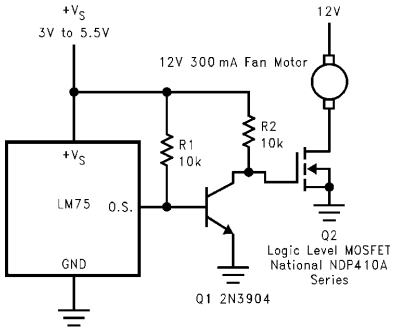
The LM75 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.2˚C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM75 die would be at an intermediate temperature between the surface temperature and the air temperature.

The path of best thermal conductivity is between the die and the GND pin, upon which the die is mounted. The printed-circuit board lands and traces connecting to the LM75 will be the object whose temperature is being measured.

In probe type applications, the LM75 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM75 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM75 or its connections.

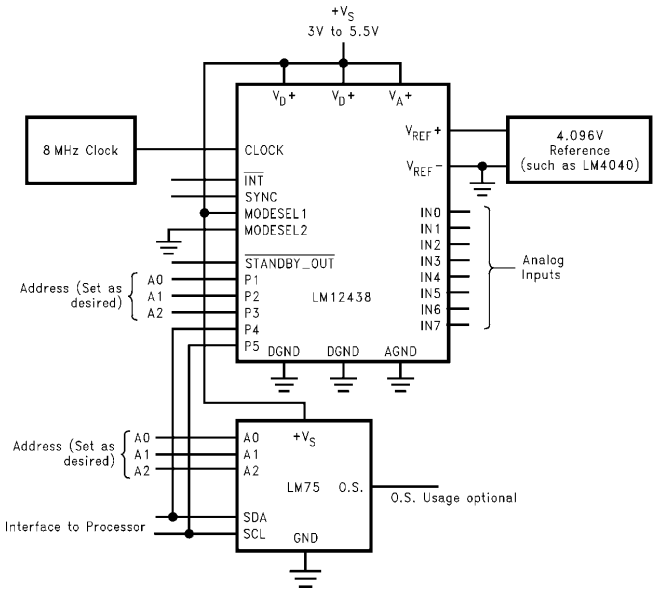
## 4.0 Typical Applications




DS012658-12

When using the two-wire interface: program O.S. for active high and connect O.S. directly to Q2's gate.

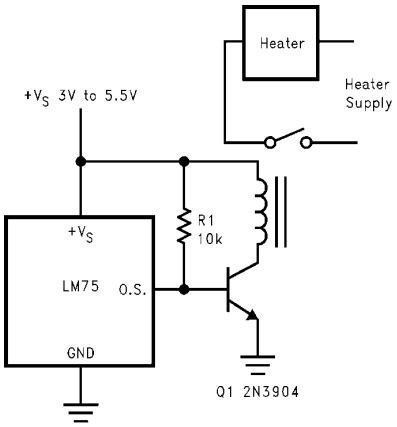
**FIGURE 8. Simple Fan Controller, Interface Optional**




DS012658-13

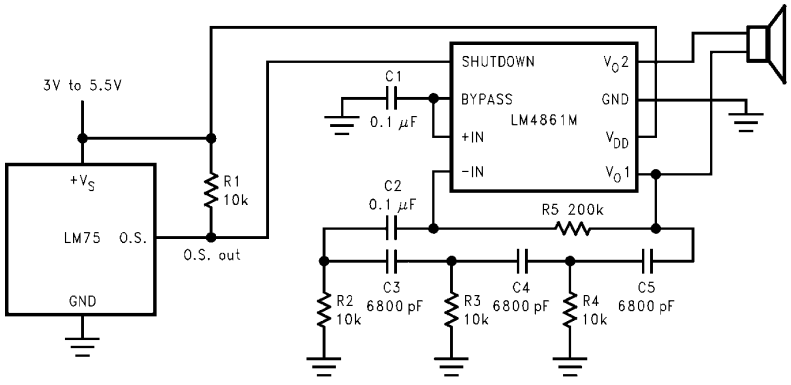
**FIGURE 9. Data Acquisition System with Temperature Input via $I^2C$ Bus**

## 4.0 Typical Applications (Continued)




DS012658-14

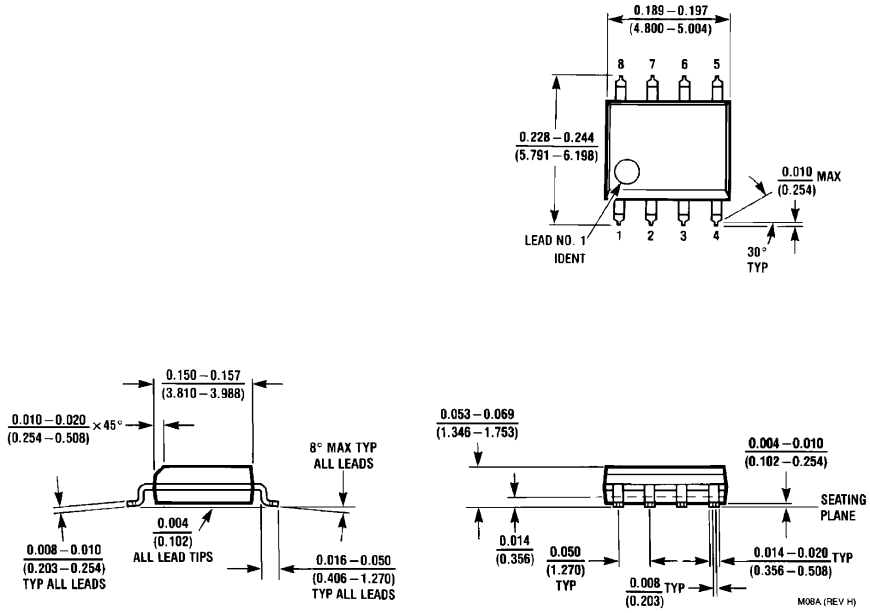
**FIGURE 10. Simple Thermostat, Interface Optional**




DS012658-15

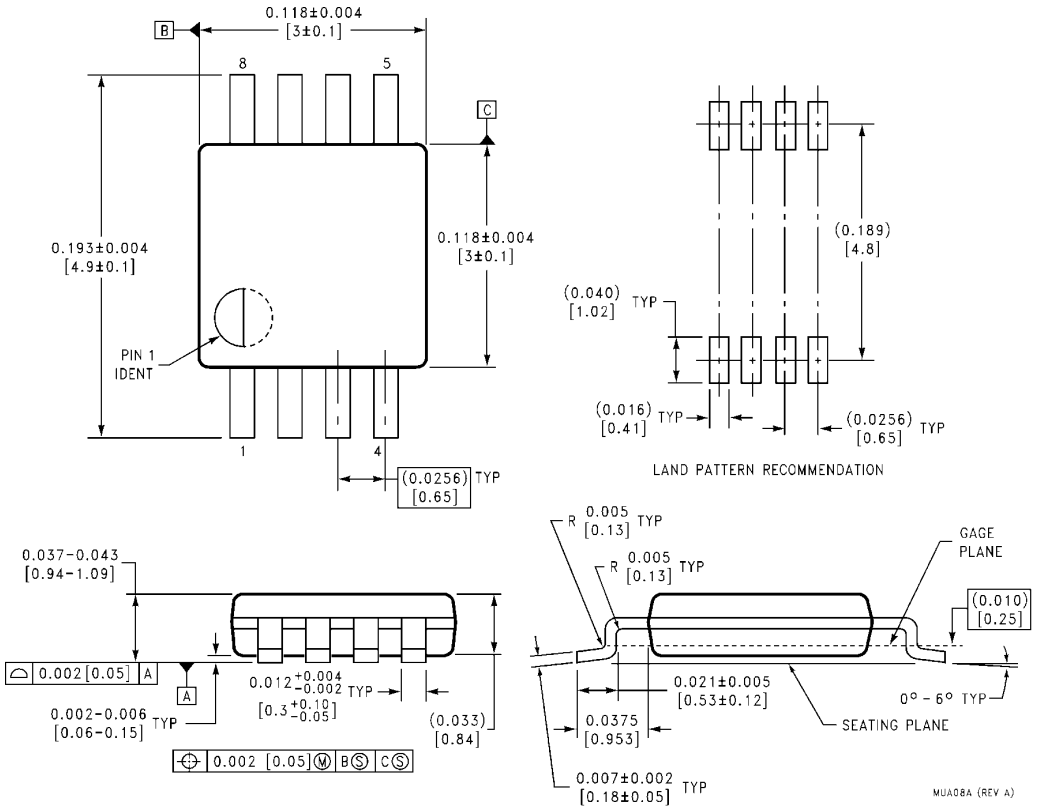
**FIGURE 11. Temperature Sensor with Loudmouth Alarm (Barking Watchdog)**

## Physical Dimensions inches (millimeters)




**8-Lead (0.150" Wide) Molded Small Outline Package (SOP), JEDEC**
**Order Number LM75CIM-3, LM75CIMX-3, LM75CIM-5 or LM75CIMX-5**
**NS Package Number M08A**

## Physical Dimensions inches (millimeters) (Continued)




**8-Lead Molded Mini Small Outline Package (MSOP)**
**(JEDEC REGISTRATION NUMBER M0-187)**
**Order Number LM75CIMM-3, LM75CIMMX-3,**
**LM75CIMM-5 or LM75CIMMX-5**
**NS Package Number MUA08A**

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# LM75 Partial Power Supply Shutdown Considerations

Certain power supply cycling conditions can defeat the LM75's internal power-on-reset (POR) circuit. To properly reset the LM75's internal circuitry and force the IC to start up with the default values for $T_{OS}$, $T_{HYST}$, etc. stored in its registers, the power supply voltage must fall below 150mV before returning to its nominal 3V or 5V operating voltage. If the power supply voltage falls no lower than 400mV, the LM75 effectively remains powered up and all register contents will remain intact.

Problems can occur if the LM75's supply voltage experiences a "partial shutdown", dropping to a voltage between 150mV and 400mV and then returning to the normal operating voltage. Under these conditions, the internal registers may reset properly (with the correct default values restored), or they may retain their existing contents, or they may "reset" to random values. In addition, OS or SDA may be in a low state when the supply voltage returns to its nominal value. The effect is time-dependent. Some devices may retain their previous register settings if they spend less than 1 second between 150mV and 400mV, but their register contents may be corrupted if they stay in this voltage range for a few seconds. Because the effect is unpredictable, and will vary from one device to the next, the LM75's register settings should be assumed to be corrupted whenever the supply voltage falls to the 150mV to 400mV range (Figure 1).

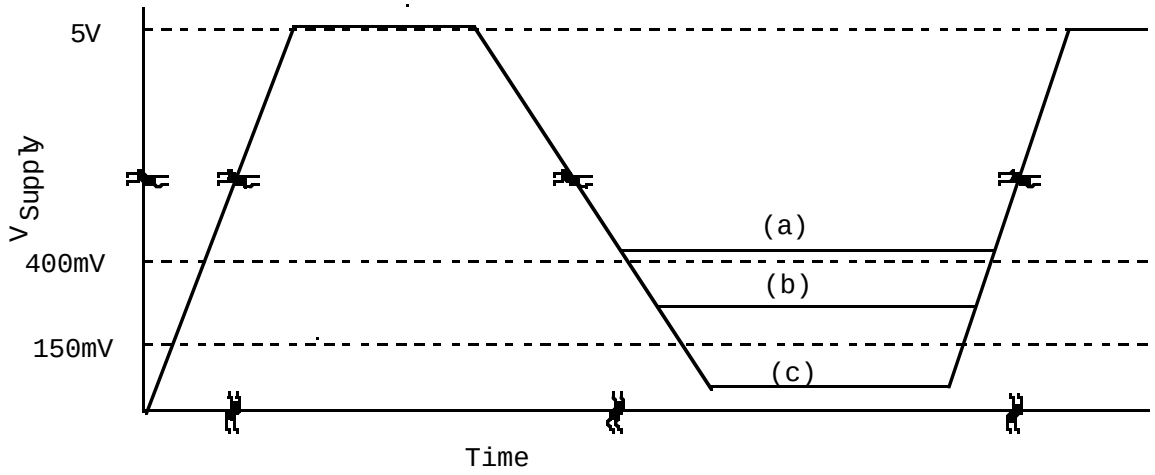


**Figure 1. Three LM75 power-cycling conditions. (a) When power is removed, the supply voltage remains above 400mV. In this case, the LM75 never resets; all data stored in memory prior to power-off is retained. (b) The supply voltage falls to a voltage between 150mV and 400mV. Data stored in memory is unpredictable and may be corrupted. (c)The supply voltage falls below 150mV. The LM75 resets properly on turn-on, and registers contain default data.**

**Causes of partial shutdown**

There are three common causes for partial power supply shutdown:

1. Fast power supply cycling due to a brief interruption in the ac mains or a user quickly toggling the system power supply switch "off" and then "on". This causes the internal supply to drop to an unknown voltage and then return to its operating value (nominally 5V or 3V).

2. Very slow supply shutdown ramp. This could be considered a subset of (1). If the system supply voltage ramps very slowly toward zero when the system is turned off, re-applying system power (even a few seconds later) can cause the LM75's supply voltage to drop into the partial shutdown region before rising back to its normal value.

3. "Residual" Supply Voltage. In some systems, even though the power supply

shuts down completely, a residual supply voltage remains. For example, when an LM75 is mounted on a PC motherboard and peripheral components (such as a monitor or printer) are connected to the system, the peripherals may force the LM75's supply voltage to a non-zero voltage if their power supplies are active while the PC is shut down.

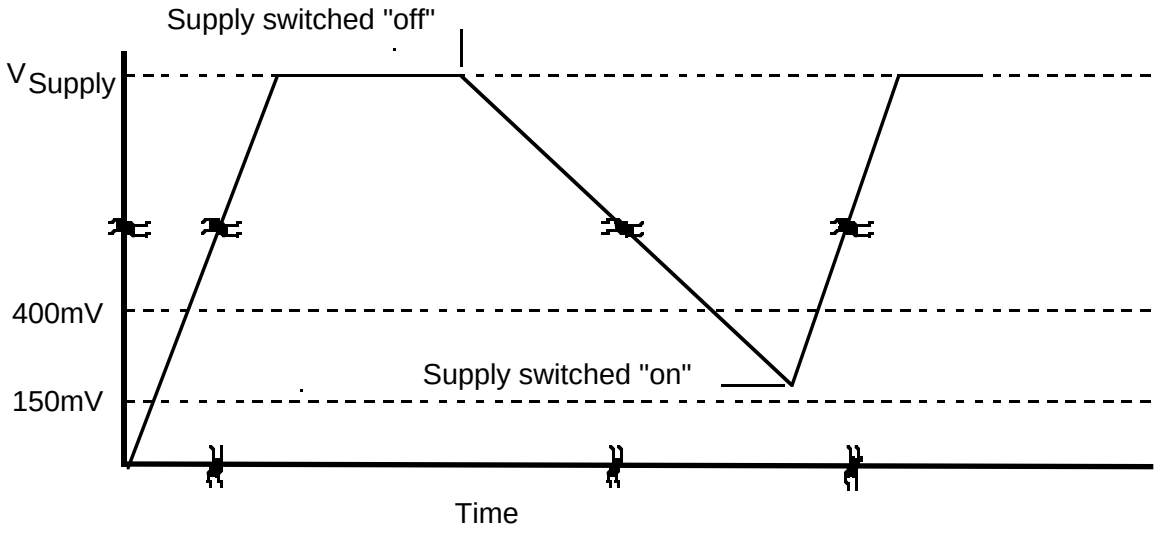


**Figure 2. Partial power supply shutdown caused by fast power supply cycling. In this case, the power supply was switched off, and then switched on again before it was able to decay to 50mV.**

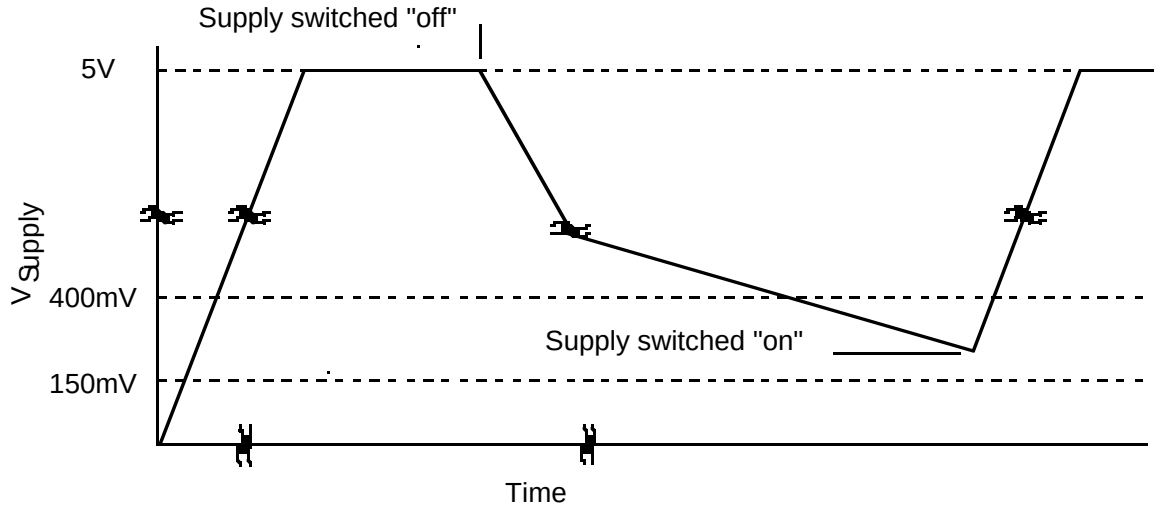


**Figure 3. Partial power supply shutdown due to a slow supply discharge ramp. After several seconds have elapsed, the supply still has a residual voltage greater than 150mV.**

**Partial Shutdown Scenarios**

Following are a few scenarios in which an LM75 may start up in an incorrect state due to a partial power supply shutdown.

**0.** Conditions: Register contents corrupted, O.S. unused or driving an interrupt input, SDA inactive.
Result: Normal system operation.

In many systems, a stand-alone Power On Reset IC restarts the system after a power interruption and O.S. drives an interrupt input that alerts the system of a temperature "event". When the system restarts, it communicates with the LM75 over the $I^2C$ interface and resets all of the LM75's registers to the required values as part of its normal start-up routine. The LM75 behaves as expected and no problems occur even if the supply voltage underwent a partial shutdown.

**1.** Conditions: O.S. unused or driving an interrupt input, LM75 pulls SDA low, Bus master with error recovery.
Result: Normal system operation.

If a partial shutdown event causes SDA to go to an active "low" condition, the newly-reset $I^2C$ bus master will interpret this a bus contention, and will not initiate communication with the LM75. If the LM75 holds SDA low for a prolonged period, an intelligent bus master (either a dedicated IC or a microcontroller) recognizes this condition and forces the LM75 to release SDA. Normal operation then resumes, beginning with resetting the LM75's registers.

**2.** Conditions: O.S. unused or driving an interrupt input, LM75 pulls SDA low, No $I^2C$ recovery capability in bus master.
Result: Communication with LM75 halts, incorrect interrupts may be generated.

If the bus master has no error recovery capability and can't restart communications when the LM75 is pulling SDA low, communication with the LM75 will halt. The O.S. output is still capable of generating interrupts, but the temperature at which this happens will be unpredictable because the threshold register contents are unknown.

**3.** Conditions: O.S. directly shuts down system power or clock at high temperatures.
Result: System will not start up.

If the LM75 is used in such a way that it can disable the system before an $I^2C$ communication can occur, a partial shutdown could prevent the system from booting. An example of this would be a PC motherboard where the LM75's O.S. output directly disables the microprocessor. If a partial shutdown causes the LM75's $T_{OS}$ threshold to be randomly set to 0°C, for example, O.S. will be low at startup (assuming the system's temperature is greater than 0°C). Since O.S. directly disables the microprocessor in this case, the system will never boot up. Similar results can occur if the LM75's O.S. output disables the system clock or some other vital signal or component.

## Solutions

1. As mentioned above, the simplest solution for scenario 1 is to use an $I^2C$ controller with error recovery. If a general-purpose device (e.g., a microcontroller) performs the $I^2C$ communications, it can clear a low SDA by simply applying 27 clock pulses to the SCLK (this is the maximum number of clock pulses necessary to clear SDA). The master can now initiate a communication by pulling SDA low. The master now has control of the bus and normal operation can resume, beginning with placing the LM75 in the "shutdown" mode, then returning it to active mode, then updating its register contents to the correct values.

2. When an $I^2C$ controller does not have a robust error recovery capability, the system may still be able to recover if an unused open-drain output is available on a general-purpose microcontroller or other component. The system must first recognize that there is an $I^2C$ communications problem. At this point, the general-purpose output (which should be connected to the SCLK line) can begin clocking the LM75 until SDA clears. Again, 27 clock pulses will ensure that SDA clears.

3. Using OS to completely disable vital components should be avoided when the LM75 will be subjected partial power supply shutdown conditions, because this could render the system incapable of recovering from an incorrect $T_{OS}$ threshold.

Instead of using the LM75 to disable the system clock to reduce power dissipation, an alternative might be to reduce the clock speed to a value low enough to substantially reduce power dissipation, but high enough to allow (slow) communication with the LM75 to reset its default values, go into shutdown mode, and return to active mode.

One way to avoid POR problems with the LM75 is to ensure that its supply voltage drops to zero when the system is switched off. If it is impossible to reliably force the system's supply voltage to zero during power-down, an alternative may be to add a few components to force the LM75's supply voltage to zero. An example is shown in Figure 4, which uses a PNP transistor as a switch between the LM75 and the power supply. The diode and resistor between the base and ground keep the transistor saturated when the supply voltage is greater than about 1V, depending on temperature.

Conversely, the LM75 will completely reset any time the supply drops below this level. It is possible to have an improper reset when the supply voltage is toggled on and off rapidly, but the probability of this happening is very low because the window of time during which the system would have to be restarted is very narrow. For example, in a system whose power supply shuts down in 200ms, the system might have to be powered up 150ms ±15ms after power was removed to cause an improper reset. If the supply drops below about1V, the LM75 will correctly reset. If you would like reset to occur at a higher voltage, add another diode in series with the one shown. The 20kΩ resistor helps to discharge the LM75 supply bypass capacitor and ensure that the supply voltage drops quickly after the LM75 ceases to draw appreciable current.

An even better solution is to power the LM75 by a PNP or p-channel FET that is driven by the system's POR IC as shown in Figure 5. This will provide a consistent, reliable shutdown and reset of the LM75. If a logic gate is available that is capable of sourcing 1mA with less than 100mV of voltage drop, the gate can replace the transistor in Figure 5.

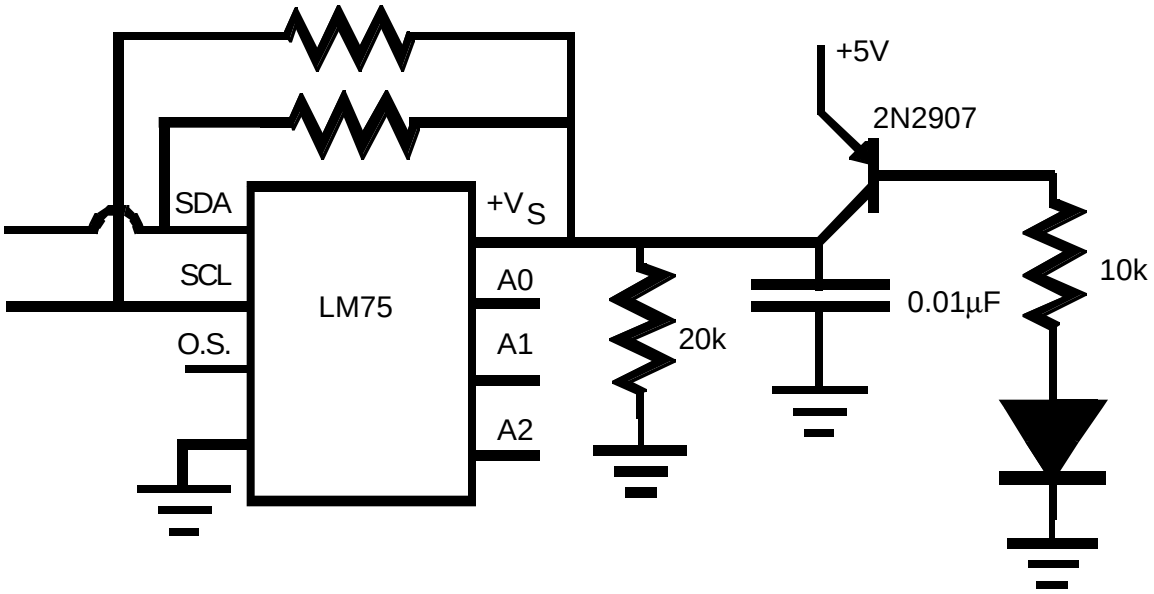


**Figure 4. This circuit will force the LM75 to reset if the supply voltage drops below about 1V.**

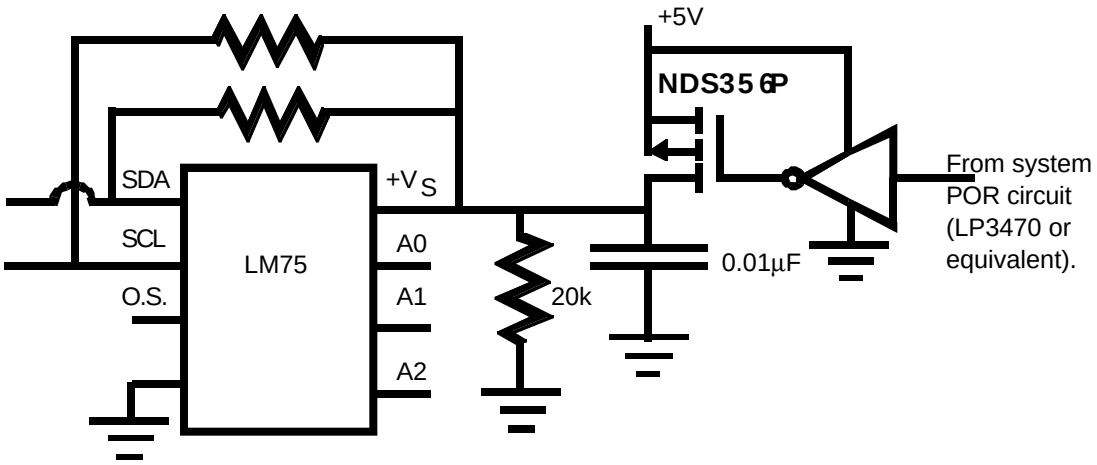


**Figure 5. This circuit provides a clean power down and reset for the LM75 whenever the system's power-on-reset circuit resets the other circuitry.**